STABLE 2 STAGE CMOS AMPLIFIER

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by

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APPROVAL AND DECLARATION SHEET

This project report titled Stable 2 Stage CMOS Amplifier was prepared and submitted by Ahmad Zainodiar Bin Khalidi (Matrix Number: 041030037) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in University Malaysia Perlis (UNIMAP).

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IC	Integrated Circuit
VLSI	Very Large Scale Integration
μ	Mobility of charge
L	Effective channel length
W/L	Aspect ratio
V_{TH}	Voltage threshold
Cox	Total capacitance per unit length
gm	Transconductance

2 PERINGKAT CMOS PENGUAT STABIL

ABSTRAK

Dalam beberapa tahun kebelakangan ini, telah ada satu usaha bagi menghasilkan produk berasaskan teknologi peralatan. Komponen kritikal yang diusahakan dalam system ini adalah sebuah penguat. Reka bentuk 2 peringkst penguat merupakan langkah yang digerak kerjakan bagi mendapatkan keluaran yang stabil apabila diberikan beban kapasitif yang berbeza. Projek ini dijalankan dengan menggunakan topologi penyelarian. Teknik ini digunakan untuk mengoptimakan keberkesanan penguat itu khususnya offset voltan dan litar biasing. Litar ini menggunakan teknologi 0.35µ dengan penggunaan arus sebanyak 110µA. Perencanaan projek ini telah menggunakan perisian Mentor Graphic bagi menguji dan merekabentuk layout. Untuk perencanaan reka bentuk layout, teknologi TSMC telah digunakan. Menggunakan penyelarian bagi mengoptimakan litar, penguat fasa boleh dikawal. Di dalam perlaksanaan CMOS penguat, terdapat batas-batas kemampuan penguat yang terhad kepada voltan keluaran tinggi dan offset voltan. Voltan yang terhasil daripada perlaksaan ini dijangka menghasilkan keluaran yang stabil.

ABSTRACT

In the last few years there has been an effort to integrate electrochemical instrumentation. A critical component of such a system is an amplifier. These projects design a “Stable Two stage CMOS amplifier”. This is achieved through the use of an optimized cascaded compensation topology. A new shifting technique allows independent optimization of drive capability, noise and systematic offset voltage. The circuit is in a 0.35µm technology and has a quiescent current consumption of 110µA. This designing currently using Mentor Graphic software to test the schematic and also to design the layout. The design layout is designed using rules from TSMC. Using cascoded compensation with optimized circuit parameters, the worst case phase margin of the amplifier can be controlled to acceptable values. In two stage CMOS amplifier, there is usually a tradeoff aware high output drive capability and low systematic offset voltage. The output voltage that expects to get must in stable conditional and the bias current setting according to the calculation estimation.