CHAPTER 1

INTRODUCTION

This chapter describes briefly about the project title, background of the project, objectives, scope of the project and the organization of the report. It consist of four sub divisions, which are project overview, project background, project specification and project organization.

1.1 Project Overview

"VGA Ball" is one of a logic digital system designs that uses source code or written program to generate it. The aim of this project is to produce a program that enables to display a "ball" that bouncing up and down the monitor. It is a rapid prototype digital design with the implementation of field programmable gate array (FPGA). Other than that, it is also applies the technology of Video Generation Array (VGA). This project proves how a written digital source code design can combine with a peripheral device (electronic monitor) to produce a video image.

As an electronic engineering student, the topic "VGA Ball" is suitable because it applies the fundamentals of logic digital system designs. Furthermore, this topic is related with subjects from previous semesters. A strong basic of programming and the knowledge of digital electronics is a must in order to precede this project. This project is

also reliable because the scope is simple, making it possible to complete in one semester.

1.2 Project Background

This project is a rapid prototype digital design with field programmable gate array (FPGA). Rapid prototype design can be defined as a group of techniques used to quickly fabricate a scale model of a part or assembly using three-dimensional computer aided design (CAD) data [11]. Digital designs is often implemented using software. Such ways to implement a digital design is either by graphical entry (logic gates level) or HDL model. This project is realized by using VHDL entry, using Quartus II Design Software.

FPGA is a type of programmable logic devices (PLD), unlike the fixed function devices, PLD have the potential to implement a broad range of functionality. FPGA is chosen from all other programmable logic devices like PLD or CPLD because of the advantages that it offers[5].

Within a digital design field there are three basic types of devices: logic, memory and processors. With recent FPGA, architectural evolutions and ever-increasing capacity, it is possible and affordable to implement all three of these elements within FPGA devices. Furthermore, FPGA become more attractive for cost-effective design prototyping based on technology advantages including: design cycle flexibility, reduced cost design iterations, low “non-recurring” (NRE) fees, the ability to easily evaluate and implement alternate design architecture, and ability to accelerate time to market for new products[4].

Before FPGA are invented, such way to implement a digital logic designs is by using the traditional integrated circuit chips, such as SSI and MSI TTL. It is obvious that the standard logic IC chips is limited to perform a fixed operation that only defined

by the manufacturer. Therefore, many programmable logic devices are invented to meet user specification. Other ways to implement a digital logic designs are the ASIC and full custom VLSI development. ASIC (Application Specific Integrated Circuits) is also an integrated circuit which internal functional is defined by the user. However, ASIC require a final customized manufacturing step. The full custom VLSI development of a design at a transistor level can require several years of engineering effort fro deign and testing. Such examples are including microprocessors and RAM chips uses in PC[1]. The designs tradeoffs of different technologies are seen in Figure 1.2.

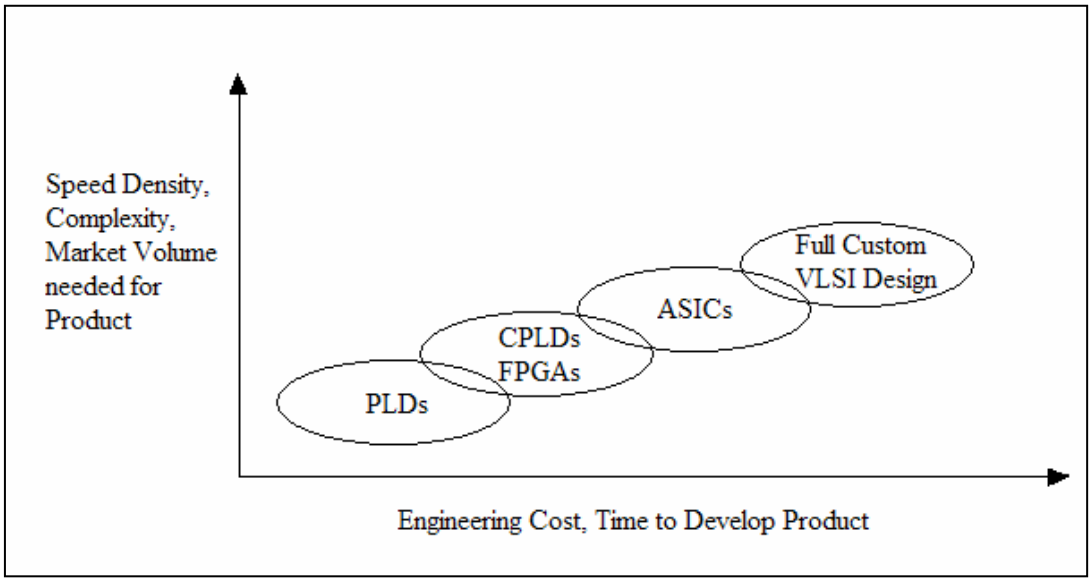

Figure 1.1 : Digital logic technologies tradeoffs [1]

The advantages of using FPGA are it have the highest density, highest speed and available at a reliable cost. Designs using FPGA typically require several weeks of engineering effort instead of months[1].

1.3 Project Specification

As mentioned earlier, methodologies that applied for this project including both High Description Language (HDL) implementation and hardware implementation. HDL implementation is which a written source code is produced to generate desired program and to realizing the HDL stage Quartus II Design Software is used. The hardware implementation is including the usage of Field Progammable Gate Array, (FPGA) board and any computer monitor that supports VGA. FPGA board is used to read and interpret the written source code and connects the resulting output to the VGA monitor. In short, the workflow of a simple digital design can be summarizes as in Figure 1.2:

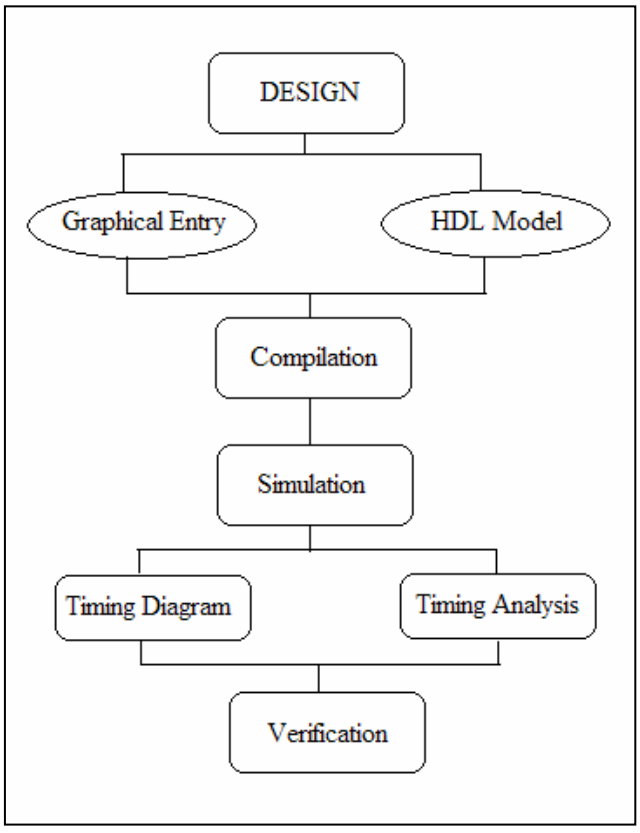

Figure 1.2: Design process for schematic or HDL entry

1.4 Project Organization

This report is organized into five chapters and each chapter contains information of this project.

(1) Chapter 1: Introduction - The first chapter described the introduction and objectives of the project. The introduction contains overview of the project, project background that explains briefly about FPGA, and project specification which explains overall methods that being used.
(2) Chapter 2: Review of Literature - Covering all literature review about the title such as VGA technology and history, Altera UP2 board, and VHDL.
(3) Chapter 3: Materials and Methodologies – Contains the methods that being used in completing this project, such as overall methods, HDL implementation and hardware implementation.
(4) Chapter 4: Results and Simulation - Contains the results simulation and discussion.
(5) Chapter 5: Conclusion - Last chapter in this report describes the conclusion of this project. It was discussed the produced result with the expected result and how the simulation can be very important to ensure the studies made.