CHAPTER 5

CONCLUSION

5.1 Summary

"Design of voltage control oscillator (VCO) in 0.18u CMOS" poses the need to operates with low power supply voltage and suitable current biasing, favorably with V_{DD} = 3.3V, and IBIAS 0.6mA. This IC process technology has been driving done the maximum allowable supply voltage. With analog circuits when reducing the supply voltage its also reduces the dynamic range and speed. So to maintain the same performance more power is consume. Another problem with reduced supply voltage is that many of the conventional analog circuit topologies will not operate anymore due to the fact that as the maximum allowable supply voltage skills down with the minimum feature size, the same amount of reduction does not happen with the threshold voltage of MOS-transistors because of increased leakage currents. The designing are basically using the cascade technique and the fundamental of this project is base on the second order effect of the MOS transistor structure. There are also the errors dealing with TSMC rules. It is because from the layout the bulk-driven normally will supply to V_{DD}. So it will covered by nwell select. But in this designing process, the designing dealing with bulk that separated supply with according to the parameter that used. To supply the bulk, it is according to V-Bulk estimation based on calculation. The problem is the rules cannot accept the rule which is bulk does not covered by nwell select. Actually, this design makes the bulk as the port connection.

5.2 Recommendation for future project

In this project, “design of voltage control oscillator (VCO) in 0.18u CMOS” using 4 stages oscillator design approach with more biggest application as CMOS amplifier, CMOS amplifier comparator and the receiver systems.. During designing this application there are difficulties occur with lower voltage supply. For example the limit of the amplifier in low power supply voltage is related to the desired input common mode range. Normal methods of designing OP-AMP can be used with care. So, in future planning the design want to test at the two stages CMOS amplifier that using low voltage supply. This is because want to test design circuit if it is function when apply to biggest circuit applications.

Thus also in future that it can make another improving circuit using low noise. This is because it very important in application where a large dynamic range is required. The dynamic range can be expressed as the ‘signal to noise ratio (SNR)’. The significant of dynamic range can be appreciated when considering the dynamic range necessary for signal resolution in terms of digital bits. In addition to noise as a lower limit, want must also consider the linearity of the circuit. If the circuit is non-linear, than a pure sinusoidal signal will generated harmonics. If the total harmonics distortion of this harmonics exceeds the noise, than non-linearity becomes the limiting factor.

The third improving planning is to approach and improving frequency compensation technique. This technique is in terms of its frequency and noise characteristic follow by its implementation in all nwell CMOS process. The technique is based on removing the feed forwardpath from the circuit at first stage output to next circuit output.

5.3 Commercialization Potential

Regarding to design of voltage control oscillator in 0.18u CMOS using cascade technique, this design have well innovative to applying technology at Antenna Receiver Subsystem (ARS). This ARS is involving through the usage of system such as the wireless Lan communication or in RF Communication as it main objective where the antenna subsystem to ability of receiving signal in wireless communication. Therefore by applying design of voltage control oscillator at RF amplifier will reduced the power consumption. Currently this ARS power consumption the amplifier about 30mW but by using this technique; the amplifier can drive 20mW of power.. These innovative applying will significantly make less money and environmental the ARS.