CHAPTER 1

INTRODUCTION

1.1 Overview

Final year project (FYP) titled, 'Design Voltage Control Oscillator' was selected because it is a famous titled that deal with reduce power and voltage with increased frequency oscillate to fulfill of requirement of integrated circuit design today. The CMOS oscillators need at least three inverters in the loops. It is guaranteed that the loop gain will still be greater than unity when the phase shift around the loop becomes greater than 180°.

1.2 Project Objective

The objective of this project is to study the voltage control oscillator and design a new type of VCO that changes in specification such as power dissipation, voltage supply and frequency.

1.3 Scope of Study

The scopes of study are to understand flow of design using CMOS technology use mentor graphic software. Also to reach the specification of power consumption and voltage supply.

1.4 Expected Finding

Voltage-controlled oscillators (VCOs) are critical building blocks in phase-locked loops (PLLs), clock and data recovery circuits (CDRs), which are widely used in wireless and wire-line communication systems. Designing VCOs for monolithic integration is always desirable but most challenging. It has to achieve high frequency operation with reasonable power consumption. In addition, the phase noise performance is also important. Finally, small chip area is essential to monolithic system integration[1].

In recent years, the CMOS oscillators have shown an excellent phase noise performance with low power consumption because of a relatively high quality factor. However, the limited tuning range and large chip area have become critical drawbacks in VCOs. On the other hand, the ring VCOs exhibit several attractive features such as the wide frequency tuning range, the ease of integration with digital CMOS process, and the small chip area. Moreover, ring oscillators generate both in-phase and quadrature-phase outputs with an even number of delay cells.The oscillation frequency of the ring oscillator is inversely proportional to the number of delay stages, N. Employing fewer delay stages can also reduce the power dissipation, chip area and cost. The minimum number of stages for quadrature outputs is N = 2. Hence it is desirable to design a two-stage ring VCO. However, in order to satisfy Barkhausen's criteria, an additional phase shift is required in each delay cell [1]. The VCO performance in terms of phase noise, tuning range and power dissipation determine many of the basic performance characteristic of a transceiver. In practice, as the oscillation amplitude increase, the stages in the signal path experience nonlinearity and eventually "saturation" limiting the maximum amplitude. The poles begin in the right half plane and eventually move to the imaginary axis to stop the growth. If the small-signal loop gain is greater than unity, the circuit speeds must have enough time in saturation so that the average loop gain is still equal to unity.

1.5 Organization of Work

Having explained the aims and design consideration of the project, further discussion upon the project will be discussed by the author in later sections. Here is a brief summary of the contents in this report.

In **Chapter 2** provides history of VCOs designed by Dr. Dan Boye and VCOs in application of amateur radio band. Basic operations for voltage control oscillator were also presented here. Factor that determine the quality of a VCO was included. Some advantages of using CMOS design compared by using old method were also presented. Three scopes of study interested to investigate the performance on VCO design waveform characteristic, frequency range and power consumption.

In **Chapter 3** describes methodology of design flow; start with netlist creation text editor netlist, simulate it from command prompt and then view and analyze the waveform results using Waveform Viewer, Using the Design Architect IC tool to design a circuit base on the given schematic and simulate it, lastly analyze the waveform result using Waveform editor. Besides that methodology on creating the layout for the circuit base on schematically design rules, running the DRC to identify and fix the errors in layout and lastly running LVS to identify and fix errors on layout and schematic are described in detail.

In **Chapter 4** presents and highlights the results and discussions obtained from methodology provided in Chapter 3.

Lastly,in **Chapter 5** presents and conclude the result of design VCO also included the problems occurs along design and simulate VCO in progress. This chapter provides a few recommendartions for future project will be discussed.