

## **CHAPTER 3**

### **METHODOLOGY**

#### **3.1 Overview**

This chapter provides methodology for design flow and method using for design voltage control oscillator on six different part that related between one and each other. Firstly, netlist are create using text editor netlist. Netlist that was simulate through command prompt can be view using waveform viewer. Using the Design Architect IC tool, schematic of voltage control oscillator are create. Waveform are analyze using waveform editor. Nest step is create layout base on schematic design rules. Running the DRC to identify the erros and try to fix it. Lastly, the process of LVS. It for identify and fix errors on layout and schematic also will be explain in detail here.

First part is design schematic follow the rule and value that been calculated before and set the value of length and width for transistor PMOS n NMOS. Second part is analysis the waveform from result of simulate the schematic. After that, the important part is tuning the bias voltage, and the value of resistance to get result same as theory. Tuning part is the very important part for this project because from this part observation will be make either this project is success or failed.

The manufacturer design could be done by using special software such as Mentor Graphic software. The technology that been used is the TSMC035 (Taiwan Manufacturing Semi Conductor Company).

### 3.2 Circuit Description

Design schematic in figure 3.1 has designed using the value calculated in part design specification. This schematic is included two part, the biasing circuit and other part is oscillator circuit. For biasing circuit the value of  $V_{bias}$  have been tune to 0.689V to get a suitable waveform.  $V_{dd}$  is set to 3.3V because for lower value than 3.3V circuit cannot be drive.  $M_3$  and  $M_4$  operate in the triode regions, each acting as a variable resistor controlled by  $V_{bias}$ . As  $V_{bias}$  become more positive, the on resistance of  $M_3$  and  $M_4$  increases, thus raising the time constant of the output and the lower value of  $f_{osc}$ . The output of VCO will go through to the input of the PMOS to get the oscillation at the output waveform. Before design of layout was done, the resistor is changes to PMOS transistor form and act as transistor. Calculation has done to get a length and width for PMOS to act as a resistor.

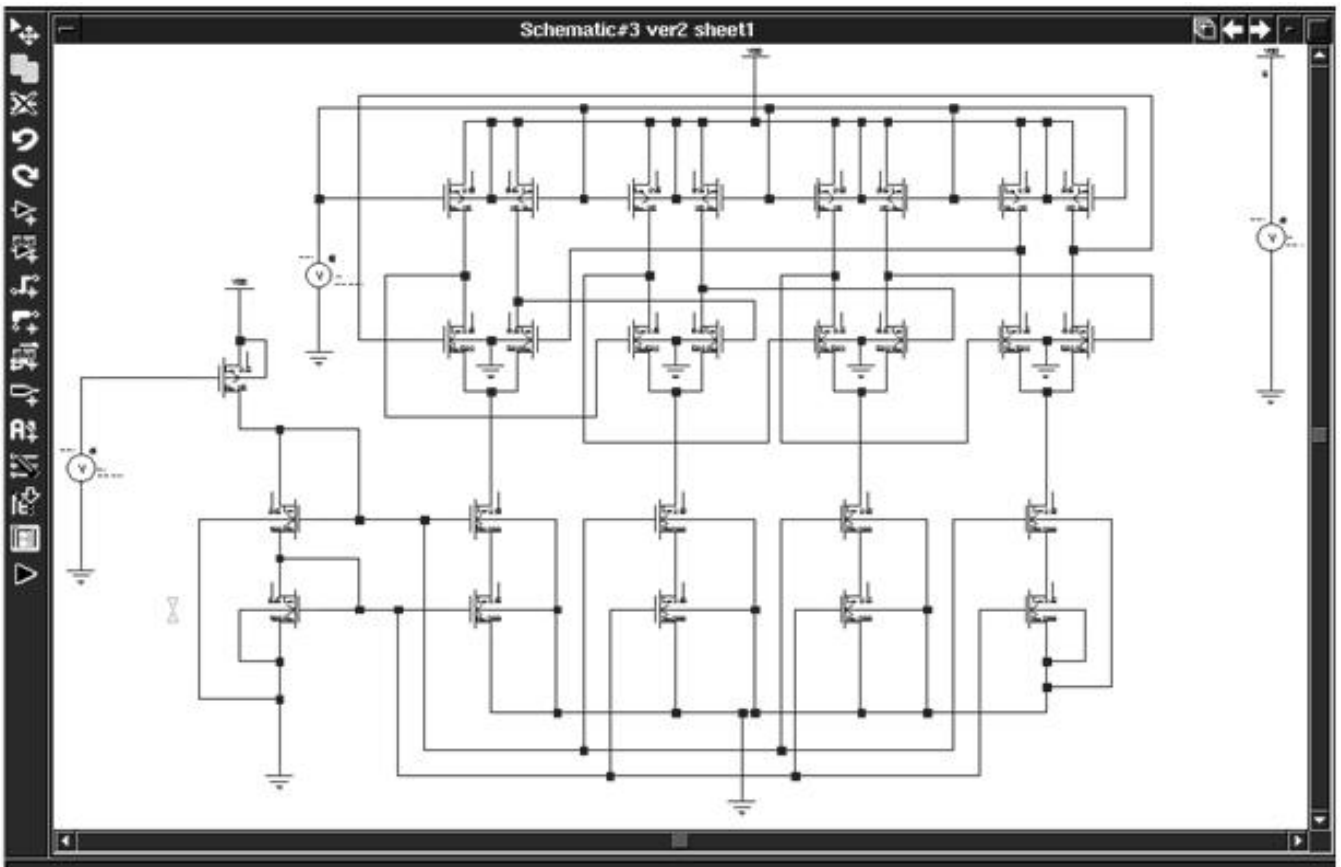


Figure 3.1: VCO Design Schematic Diagram

Cascade technique are apply to design the voltage control oscillator.,observation that either the circuit can drive low voltage by using the cascade techniques. Actually from the calculation value,it was to compare either it is different than the practical value. To get the exactly value,  $V_{GS}$  has tuned base on calculation. Then, analyzed the waveform from waveform editor. The output must be stable according to the project objective. If  $I_{REF} = I_{OUT}$ , the  $V_{GS}$  will be tuned based on calculation guideline.

### **3.3 Design Specification**

To reach the objective of the project certain specifications must be follow to get optimum result.

#### **3.3.1 Specification**

Base on design specification, the design supplied by 3.3V  $V_{DD}$ . The power consumption is 20mW has been set up. According to the calculation, the powers are just assuming about 40% only. This is because in the real situation, the power cannot get 100% the real value.. So 40% is the suitable value for this design. The parameters  $\mu_n$ ,  $\mu_p$ ,  $C_{OX}$ ,  $V_{THN}$ ,  $V_{THP}$ ,  $\gamma_P$ ,  $\gamma_n$ ,  $2\phi_F$  are defined from MOS Spice Models [5].

#### **3.3.2 Design Approach**

Regarding from this design, the value  $V_{GS}$  is very important to adjusting the circuit to get output in stable mode. Thus the  $I_{bias}$  must be calculate from triode region where the power consumption has been set to 20mW. In design,  $I_{bias}$ ,  $I_{REF}$  and  $V_{GS}$  are not same value base on the  $V_{DD}$  that are supply. The value  $I_{bias}$  is will be effect to hole calculation such as size of transistor,  $V_{GS}$ , resistor and also capacitance value. Below is the calculation to start the design.

**Assume Pd** = 8 Mw (Based on 40 ~ 50 % of actual value)

$$\text{Power} = 4 I_{\text{bias}} V_{\text{dd}} = 8 \text{ mW} \quad (3.1)$$

$$I_{\text{bias}} = \frac{8\text{m}}{4(3.3)} = 0.606\text{mA} \approx 0.6\text{mA}$$

**Size of M<sub>3</sub>** =  $\left(\frac{W}{L}\right)_{M3}$  ; M<sub>3</sub> in triode region act as resistor load.

$$\text{Choose } V_{\text{DS}} = 1\text{V} \quad , \quad V_{\text{THP}} = -0.69\text{V} \quad , \quad V_{\text{bias}} = 0.65\text{V}$$

$$\begin{aligned} V_{\text{GS}} &= V_{\text{G}} - V_{\text{bias}} \\ &= 3\text{V} - 0.65\text{V} \\ &= 2.65\text{V} \end{aligned}$$

$$\begin{aligned} \left(\frac{W}{L}\right)_{M3} &= \frac{I_D}{\mu_p C_{o_x} \left( (|V_{\text{GS}}| - |V_{\text{THP}}|) V_{\text{DS}} - \frac{1}{2} |V_{\text{DS}}|^2 \right)} \quad (3.2) \\ &= \frac{0.606\text{m}}{150.63 \times 10^{-4} \times 4.56 \times 10^{-3} \left( (2.65 - 0.69)(1) - \frac{1}{2} (1)^2 \right)} \end{aligned}$$

$$\left(\frac{W}{L}\right)_{M3} = 6$$

We find and recalculate I<sub>DS</sub> :

$$\begin{aligned} I_D &= \mu_p C_{o_x} \left(\frac{W}{L}\right)_{M3} \left( (|V_{\text{GS}}| - |V_{\text{THP}}|) V_{\text{DS}} - \frac{1}{2} |V_{\text{DS}}|^2 \right) \quad (3.3) \\ &= 150.63 \times 10^{-4} \times 4.56 \times 10^{-3} \times (6) \left[ (2.65 - 0.69)(1) - \frac{1}{2} (1)^2 \right] \\ &= 0.601\text{mA} \end{aligned}$$

**Find the R<sub>ON</sub> for M<sub>3</sub>:**

$$R_{\text{ON}} = \frac{1}{\mu_p C_{o_x} \left(\frac{W}{L}\right)_{M3} \left( (V_{\text{GS}} - V_{\text{THP}}) - V_{\text{DS}} \right)} \quad (3.4)$$

$$\begin{aligned}
&= \frac{1}{150.63 \times 10^{-4} \times 4.56 \times 10^{-3} \times (6) [(2.65 - 0.69) - (1)]} \\
&= 2.527 K\Omega
\end{aligned}$$

**Current source ( $I_{bias}$ ) :**

$$M_8 : \text{Let } \left(\frac{W}{L}\right)_{M8} = \left(\frac{20}{0.5}\right) , \quad V_{THN} = 0.5V$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_{M8} [(V_{GS} - V_{THN})^2]$$

$$\frac{0.6mA}{2} = \frac{1}{2} \times 415.86 \times 4.56 \times 10^{-3} \left(\frac{20}{0.5}\right)_{M8} [(V_{GS} - 0.5)^2]$$

$$V_{GS} = \sqrt{\frac{2(0.6m/2)}{\mu_n C_{ox} \left(\frac{20}{0.5}\right)_{M8}}} + V_{THN} \quad (3.5)$$

$$\begin{aligned}
&= \sqrt{\frac{2(0.6m/2)}{415.86 \times 10^{-4} \times 4.56 \times 10^{-3} \times \left(\frac{20}{0.5}\right)_{M8}}} + 0.5 \\
&= 0.761V
\end{aligned}$$

$$V_{GS} = V_G$$

**Size  $M_8$  is equal with  $M_7$  ;**

$$\left(\frac{W}{L}\right)_{M7} = \left(\frac{W}{L}\right)_{M8} = \left(\frac{20}{0.5}\right)$$

$$V_{GS} = (V_G - V_S)_7$$

$$I_{D7} = 0.5M = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_{M8} [(V_{GS} - V_{THN})^2] \quad (3.6)$$

$$V_{GS} - V_{TH} = (V_G - V_S - V_{TH}) = \sqrt{\frac{2(0.3m)}{415.86 \times 10^{-4} \times 4.56 \times 10^{-3} \times \left(\frac{20}{0.5}\right)_{M7}}} = 0.281$$

$$V_{G7} = 0.281 + 0.761V + 0.5V = 1.54V$$

So,

$$R_L = \left(\frac{V_{DD} - V_{G7}}{I_{D7}}\right) = \left(\frac{3.3 - 1.54}{0.3m}\right) = 5.866K\Omega$$

**Find total capacitance :**

$$f = \frac{1}{2 \ln 2 NRC} \quad (3.7)$$

N = Number of stage

C = Capacitor if inverter stage

R = Resistance of active load

$$\begin{aligned} C &= \frac{1}{2 \ln 2(4)R_{ON3}(2.0G)} \\ &= \frac{1}{2 \ln 2(4) \times (2.527K\Omega) \times (2G)} \\ &= 35.68fF \end{aligned}$$

$$C_{total} = C_{GD3} + C_{GS16} + C_{GD1} + C_{GD16} \quad (3.8)$$

**M<sub>1</sub> and M<sub>16</sub> are in saturation so  $C_{GD1}$  and  $C_{GD16} = 0$**

$$\begin{aligned} &= \frac{1}{2}C_{ox}(WL)_3 + \frac{2}{3}C_{ox}(WL)_{16} \\ &= \frac{1}{2}(4.56 \times 10^{-3})(5.0 \times 10^{-6} \times 0.5 \times 10^{-6}) + \frac{2}{3}(4.56 \times 10^{-3})(W \times 0.5 \times 10^{-6})_{16} \end{aligned}$$

$$35.68fF - 5.7 \times 10^{-15} = 1.52 \times 10^{-9}W_{16}$$

$$W_{16} = 19.72\mu m$$

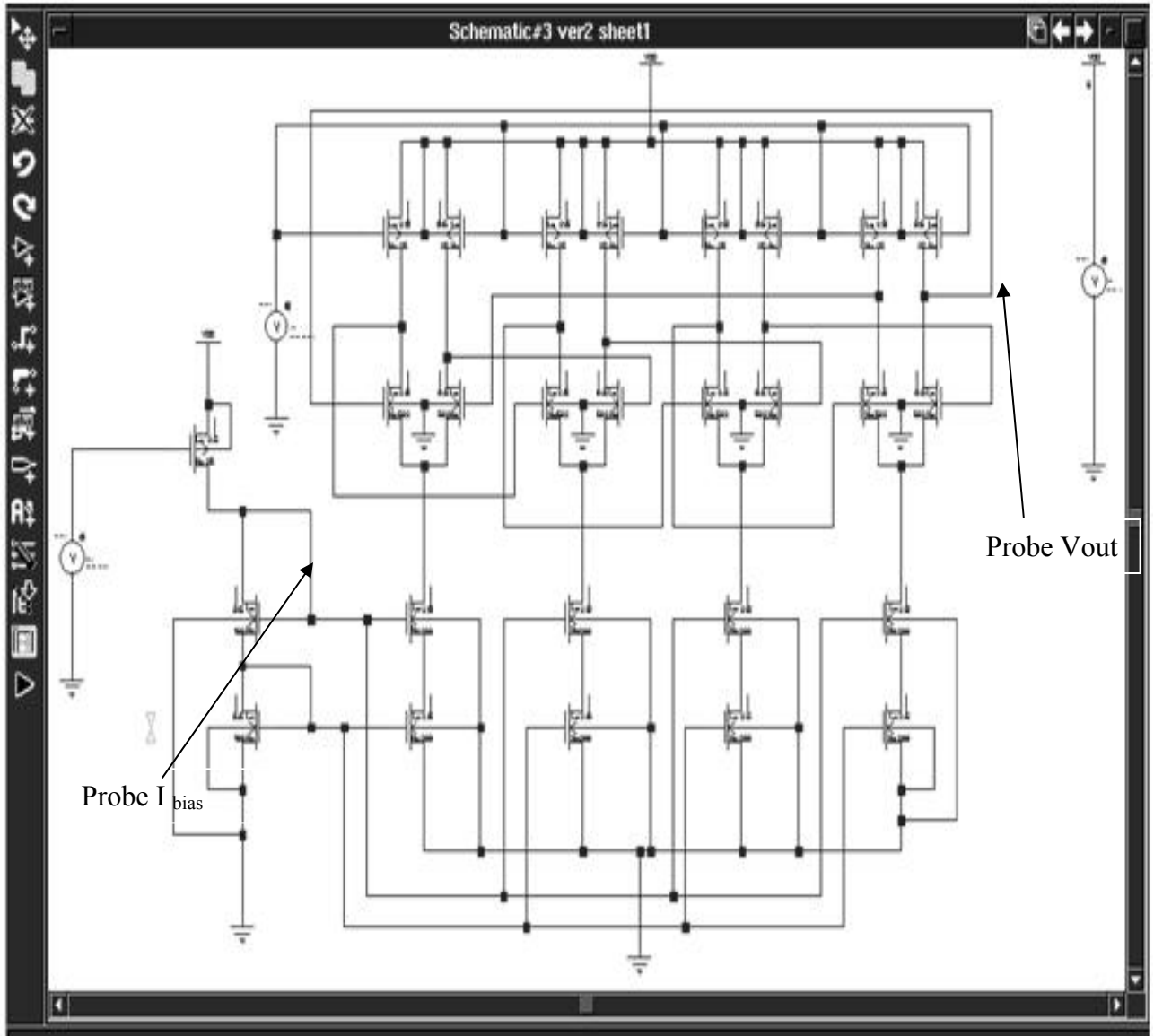
**Table 3.1:** Specification of VCO

<b>VDD</b>	<b>3.0v</b>
Power	20mW
Stage	4
$\mu_n$	415.86 cm <sup>2</sup> /Vs
$\mu_p$	150.63 cm <sup>2</sup> /Vs
C <sub>OX</sub>	4.56 x 10 <sup>-3</sup> F/m <sup>2</sup>
V <sub>THN</sub>	0.5V
V <sub>THP</sub>	0.69V
$\gamma_P$	0.4
$\gamma_n$	0.45
I <sub>bias</sub>	0.6mA
R <sub>ON</sub>	2.527K $\Omega$
R <sub>L</sub>	5.886K $\Omega$
V <sub>GS</sub>	2.65
C	35.68 fF

Table 3.1 shown the parameters and the estimation of I<sub>bias</sub>, V<sub>GS</sub> R<sub>L</sub> R<sub>ON</sub> and capacitance for V<sub>DD</sub> 3.3V.

### 3.4 Simulation

The concept of module provides the basis for hierarchical design in mentor graphic. To design the schematic, the design architecture (da) environment in mentor graphic must be used. The standard cell library with physical layout available for auto placing/routing in 'ic library'. After schematics are completed block symbol must be created to represent the circuit. This symbol can be used in other schematic to perform the same function as the original circuit. Then; the schematic is checked and saved before simulated using EZwave tools.



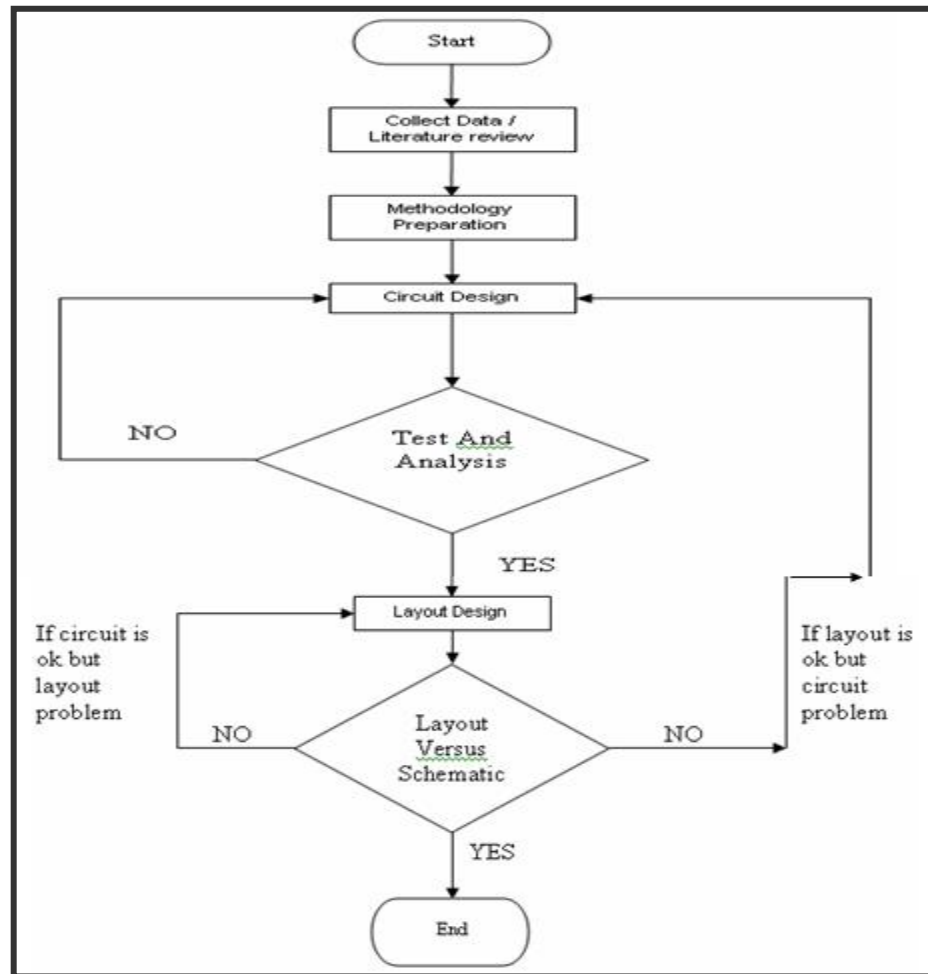
**Figure 3.2:** Probe position in circuit

Continue the simulation; probes have to place at point  $I_{bias}$  and  $V_{OUT}$  as shown in figure 3.2. So as the result,  $I_{bias}$  must be at range 0.606mA and  $V_{OUT}$  is around 2.63V If the waveform is not stables, tuning the circuit until it comes out the successfully expectation.



### 3.5 Layout

To design the layout base the schematic, the ic station software environment in mentor graphic must be used. Create the layouts by using the schematic driven layout (SDL). This technique creates ic layout from logic database information and placement done by automatically instance. The rules for the layout are ‘adk design kit TSMC0.35’. After the automatically instance, place the entire poly with the poly contact. After completely connect the poly contact, used the auto-rote technique to make connection of the layout according to the schematic logic. As the result, the layout will connect each other based on the logic schematic using metal1 and metal2. If the layout has metal3, metal4 and others, rearrange the connection to used only metal1 and metal2. Layout done, by completed with test the ‘Layout Versus Schematic (LVS)’. This testing is actually compared the netlist of the schematic to the netlist of the layout. Both netlist schematic and layout must same as shown in Chapter 4 (table (4.2) and (4.3)). The netlist of the schematic is generated in designed architecture (da) while the netlist of the layout is generated in ic station. After created the run LVS, the tools will appear the result of the comparing between layout and schematic. If there is an error, settle down the error according to transcription that appears at the result. Sometimes, once miss state in the layout will generate a few errors in LVS. So fixing one error might remove several errors from the report. Then, re-run LVS by simply clicking on icon run LVS. The report RVE we automatically update. Once all the LVS errors have been fixed calibre LVS should generated and LVS report with the smiley face. Similarly, the calibre LVS RVE window will also have the smiley face indicating that the layout is LVS clean.



**Figure 3.3:** Flow Chart VCO design

Next, test the layout using calibre ‘Design Rules Check (DRC)’. This testing is used to look for geometry based rule violations and rules are based on technology constraints. To check the DRC, we have to create a run DRC. Once the DRC is down to window will appear. One is the calibre DRC RVE window and the other is the DRC summary reports. If there is an error for the DRC, double click on the error and it will highlight the layout that shows the error. So, fix the error according to TSMC rules until DRC is clean. If there is no DRC error, the DRC summary report will indicate there are ‘0’ DRC results generated at the total DRC results generated.

All the methodology process sequence are shown in appendix B.