DESIGN OF CONTROL CIRCUIT FOR AN INVERTER

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by

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APPROVAL AND DECLARATION SHEET

This project report titled Design of Control Circuit for An Inverter was prepared and submitted by Nurfaiza Hanim Mohd Saleh (Matrix Number: 031030725) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) University Malaysia Perlis (UniMAP).

Checked and Approved by

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MEREKABENTUK LITAR KAWALAN PENYONGSANG

ABSTRAK

Tesis ini membangunkan kawalan suis fasa tunggal titian pengimbal *Sinusoidal Pulse Width Modulation* (SPWM). Teknik yang digunakan untuk merekabentuk litar kawalan penyongsang ini ialah mengunakan VHDL *programming* dan *Altera Quartus II*. Kerangka kerja utama untuk kawalan pengsuisan terbentuk di mana merangkumi penggunaan teknologi *Metal Oxide Semiconductor Field Effect Transistor* (MOSFET).Berdasarkan kepada teori, teknik pengsuisan untuk litar pengimbal diperlukan untuk menghasilkan gelombang keluaran yang hampir sama dengan gelombang sinus tulen yang dihasilkan oleh pengimbal unggul. Oleh itu, kaedah pengsuisan yang mempunyai fleksibiliti yang tinggi digunakan bagi mendapatkan pengsuisan tulen gelombang sinus *Pulse Width Modulation* (PWM) yang sempurna dari terminal keluaran litar penyongsang. Terdapat tiga bahagian litar dalam merekabentuk litar kawalan penyongsang ini, iaitu perisian, litar pengantara muka dan litar penyongsang. Simulasi digunakan untuk mengesahkan keputusan selanjutnya bagi mendapatkan keluaran asli daripada rekabentuk perkakasan. *Field Programmable Gate Array Technology* (FPGA) adalah salah satu bahagian yang sesuai dalam merekabentuk litar pengsuisan.Untuk frekuensi pengsuisan projek ini ialah 2.083 *khz* dengan frekuensi asasnya ialah *50.25 hz* adalah keluaran yang diuji daripada litar penyongsang.

ABSTRACT

This thesis develops sinusoidal pulse width modulation (SPWM) technique switching for single phase bridge inverter. This technique is design using (VHDL) programming with Altera Quartus II environment. A general framework for switching control is developed, which encompasses relevant Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Theoretically, the switching technique for inverter circuit need to produce output waveform as close as the purely sine wave as generated by the ideal inverter. Therefore, this method is developed with high programming flexibility as to accomplish purely sine wave from the inverter output terminal. Three part circuits of the design are involved software development, interface circuit and the inverter circuit. Simulations are used to further corroborate the results and done prior to the hardware design. Field Programmable Gate Array (FPGA) Technology is adapted as the part of the circuit design in order to control the switching of the inverter switches. The switching frequency of this project is 2.083 khz with the fundamental frequency of 50.25 hz out from the tested inverter.

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LIST OF SYMBOLS, ABBREVIATIONS OR NOMENCLATURE

VLSI	Very Large Scale Integration
VHDL	VHSIC Hardware Description Language
FPGA	Field Programmable Gate Array
UP3	University Programme 3
DC	Direct Current
AC	Alternative Current
UPS	Uninterreptible Power Supply
SRAM	Static Random Acsess Memory
JTAG	Joint Test Action Group
BST	Boundary Scan Test
PCBs	Printed Circuit Boards
AS	Active Serial
MSE	Mode Select Enable
CSIs	Current Source Inverters
VSIs	Voltage Source Inverters
SPWM	Sinusoidal Pulse Width Modulation
CAD	Computer Aided Design
Les	Logic Elements