CHAPTER 2

LITERATURE REVIEW

This chapter is divided by two sections. The first section discussed about the FPGA (Field Programmable Gate Array) and another section explained the inverter.

2.1 FPGA (Field Programmable Gate Array) architecture

FPGA (Field Programmable Gate Array) technology is used as main controller is this project to download the design. The applications of Very Large Scale Integration (VLSI) are getting more important and popular. Recently, microcontroller is widely used in industry and the application of this VLSI chip extended in many applications especially as the main controller for various types of controller circuit. Additionally, with the advance of power electronics technology, solid state devices such as relays and many more are replaced by the high speed power semiconductor switches. This introduced to the digital controller to replace the existing analog controller mostly in switches controlled devices. FPGA uses SRAM cells to store configuration data must be downloaded to cyclone FPGA each time the device powers up. There are three methods to configure the device active serial configuration, passive serial configuration and JTAG-based configuration. This project is used the UP3 board to download the design, where is the UP3 board had supports two modes; active serial mode and JTAG (Joint Test Action Group) mode.

2.1.1 Active Serial Mode

Active serial configuration is carried out through serial configuration device EPCS1. Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone FPGA read configuration data via the serial interface decompresses data if necessary and program their SRAM cells. These scheme is referred to as an AS configuration scheme because the FPGA controls the configuration interface. The Quartus II software automatically generates files that can be downloaded into the configuration devices using Byte-Blaster II for Active serial configuration.

2.1.2 JTAG Mode

JTAG (Joint Test Action Group) interface. JTAG has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture offers the capability to efficiently test component on printed circuit boards (PCBs) with lead tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. The Quartus II software automatically generates files that can be downloaded using Byte-Blaster II or USB Blaster Cable for JTAG configuration.

This project used the active serial mode, where is on UP3 board, active serial configuration scheme is combined with JTAG based configuration like as shown on Figure 2.1. The MSE (Mode Select Enable) pins are tied low to select the active serial configuration mode.

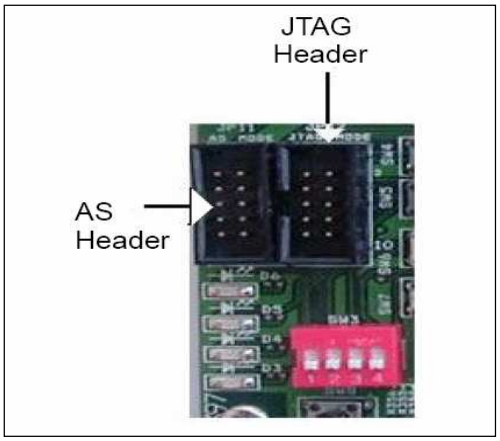

Figure 2.1: Active serial and JTAG header

This setup uses two 10 pin download cable header on the board. The first header (JP11) programs the serial configuration device in system via the active serial programming interface and the second header (JP12) configures the cyclone FPGA directly via the JTAG interface.

Table 2.1: Active Serial Header (JP11)

Header (JP11) Pin no.	Signal	EPCS1(U15) Pin no.	FPGA(U11) Pin no.
1	DCLK	6	36
2	GND	-	-
3	CONF_DONE	-	145

Table 2.1: Active Serial Header (JP11) (continued)

Header (JP11) Pin no.	Signal	EPCS1(U15) Pin no.	FPGA(U11) Pin no.
4	+3.3V	-	-
5	CONFIG#	-	25
6	CE#	-	32
7	DATA	2	25
8	CSO#	1	24
9	ASDO#	5	37
10	GND	-	-

Table 2.1 is shown the pin number for active serial header (JP11) that used for this project. U15 is a serial configuration device (EPCS1) for the cyclone FPGA on UP3 board. Serial configuration devices are flash memory devices with a serial interface that can store configuration data for a cyclone device and reload the data into the device upon power up or re-configuration.

2.2 UP3 Education Kit

Figure 2.2 are shown overview of the important components on UP3 board that used in this project.

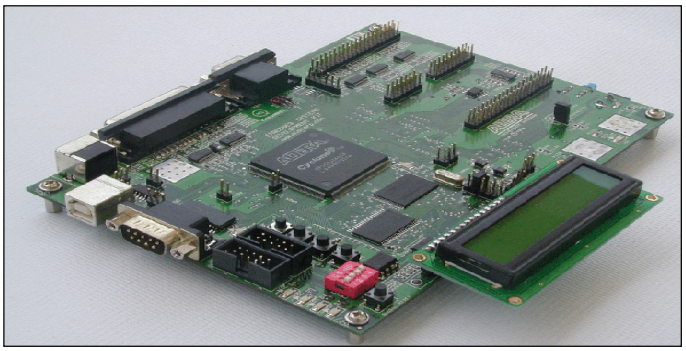

Figure 2.2: UP3 board

The UP3 Education Kit provides an educational support and also a low cost solution for prototyping and rapidly developing products. The board serves as an excellent means for system prototyping, emulation and hardware as well as software development. The UP3 board has industry standard interconnections, memory subsystem, multiple clocks for system design, JTAG configuration, and expansion headers for greater flexibility and capacity and additional user interface features.

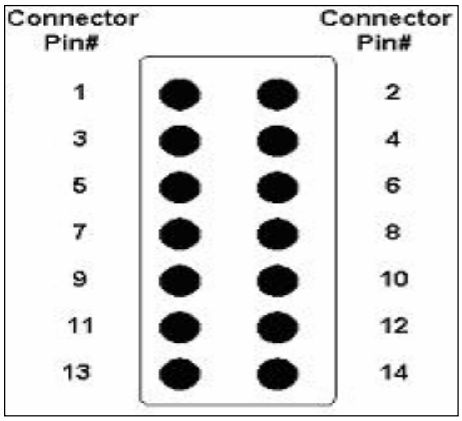

Figure 2.3: Expansion Prototype Connector-J2

Figure 2.3 is shown that the expansion prototype connector –J2 which is used in this project for the output pin. The connector of pin number and FPGA (Field Programmable Gate Array) pin number had shown like as on Table 2.2.

Table 2.2: J2 connector pin number

Connector Pin no.	FPGA Pin no.
1	GND
2	+5V
3	NC
4	186
5	195
6	185
7	194
8	184
9	193
10	183
11	188
12	182
13	187
14	198

2.3 Inverter

The function of an inverter is to change a DC input voltage to a symmetrical AC output voltage of desire frequency and magnitude. Generally, inverters can be classified into two type i.e. current source inverters (CSIs) and voltage source inverters (VSIs).

Current source inverters are useful for very high power AC motor drives where the DC input to the inverter is a DC current source. On the other hand, for the voltage source inverters, the DC input to the inverter is a DC voltage source. Voltage source inverters are categorized as square wave inverter, pulse width modulated inverter and single phase inverter with voltage cancellation. The detail explanation to be discuss in the next section.

2.3.1 Square wave inverters

These inverters use controlled DC input voltage in order to control the magnitude of the output AC voltage. The parameter controlled by these types of inverters is only the output frequency from the inverters. The output voltage from these inverters has a waveform similar to a square wave. The operation of this inverter is discussed in section

2.3.2 Pulse width modulated inverters, PWM inverters

The input DC voltage for these inverters is essentially constant in magnitude. The AC output voltage from the inverter is magnitude and frequency controllable. This is achieved by switching the inverter switches using PWM switching scheme and hence such inverters are called PWM inverters. The operation of this inverter is discussed in section 2.5.

2.3.3 Single phase inverter with voltage cancellation

These inverters are combination of the characteristics of the square wave inverters and pulse width modulated inverters. This inverter is able to control the magnitude and the frequency of the inverter output voltage even the input DC voltage is

fixed and the inverter switches are not pulse width modulated. This kind of inverter only works only with single phase inverters.

2.4 Generation of Sinusoidal Pulse Width Modulation signal

The conventional method to produce the SPWM signal is shown graphically in Figure 2.4. This method uses an analog device i.e. a comparator to generate the signal.

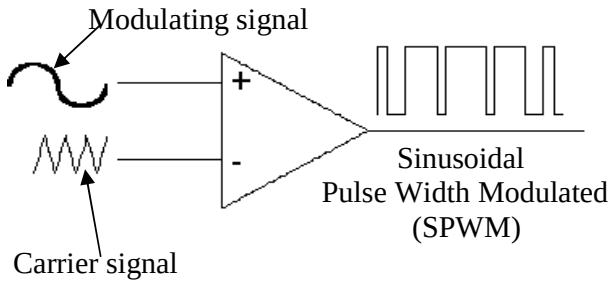

Figure 2.4: Conventional method to generate SPWM signal

Comparator is used to compare the desired reference waveform (modulating signal) with a repetitive switching frequency triangular wave (carrier signal) instantaneously as shown in Figure 2.4. The resulting waveform is depending on whether the modulating signal is larger or smaller than the carrier signal. The resulting SPWM signal with different duty cycle is also shown here. Some important definitions and considerations of this method are justified as follow:

1. Frequency modulation ratio, m_f

$$m_f = \frac{f_{tri}}{f_{\sin}} \tag{1.1}$$

Where f_{tri} = Frequency of the carrier signal

$f_{\sin}$ = Frequency of the modulating signal

Frequency modulation ratio or m_f is the ratio between the frequencies of the carrier and the reference signal where m_f is either odd or even and is usually greater than one.

2. Amplitude modulation ratio, m_a

$$m_a = \frac{A_m}{A_c} \tag{1.2}$$

Where A_m = peak amplitude of sinusoidal signal.

A_c = peak amplitude of carrier signal.

If the amplitude modulation ratio m_a is less than one, the amplitude of the fundamental frequency of the output voltage is linearly proportional to m_a. Therefore the effective AC output voltage is:

$$V_{o1} = m_a V_{DC} \tag{1.3}$$

Where V_{o1} = Amplitude of the fundamental frequency of the output voltage.

Basically, there are two types of SPWM switching scheme available i.e. bipolar and unipolar switching schemes. The Operation for each switching scheme is described in the 2.5 section.

2.5 Inverter Switching Scheme

In order to explain the operation of both bipolar and unipolar switching schemes, the basic bridge inverter circuit as illustrated in Figure2.5 is referred.

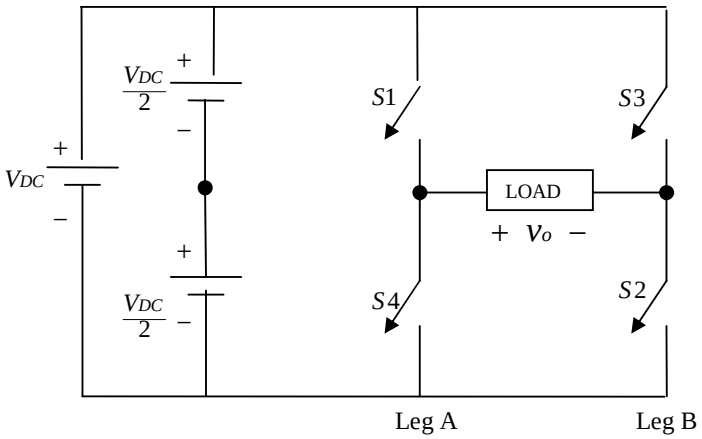

Figure 2.5: Basic bridge inverter circuit

The bridge inverter consists of four switches represented by switches S1 through S4. Leg A consists of switches S1 and S4, while leg B consists of switch S2 and S3. The switches (S1 and S2) and (S3 and S4) are operated as two pairs during switching time.

Different switching scheme produces different shape of the output voltage across the load of the inverters. The following section discussed the switching schemes and the results.

2.5.1 Square wave inverters

The control signals used to control the inverter switches is shown in Figure 2.6 (a) and (b) represented as $g1$ and $g2$ respectively. The gating signal $g1$ is used as a control signal for switches S1 and S2. While $g2$ is the control signal for switches and S3 and S4.

There are two combinations of switch on states and the corresponding voltage levels for square wave switching scheme;

During intervals of t1 and t2,

1. S1, S2 on: $v_{Ao} = \frac{+V_{DC}}{2}$, $v_{Bo} = \frac{-V_{DC}}{2}$; $v_o = +V_{DC}$

During intervals of t2 and t3,

2. S3,S4 on: $v_{Ao} = \frac{-V_{DC}}{2}$, $v_{Bo} = \frac{+V_{DC}}{2}$; $v_o = -V_{DC}$

The sequences of on and off occurred continuously and produce the output voltage from the inverter as shown in Figure 2.6(e). The output voltage has a waveform similar to a square wave, hence these inverters are called square wave inverters. The magnitude of the output voltage from the inverter with square wave operation is regulated by controlling the input DC voltage as the following equation.

$$V_{o1} = \frac{4}{\pi} V_{DC} \tag{1.4}$$

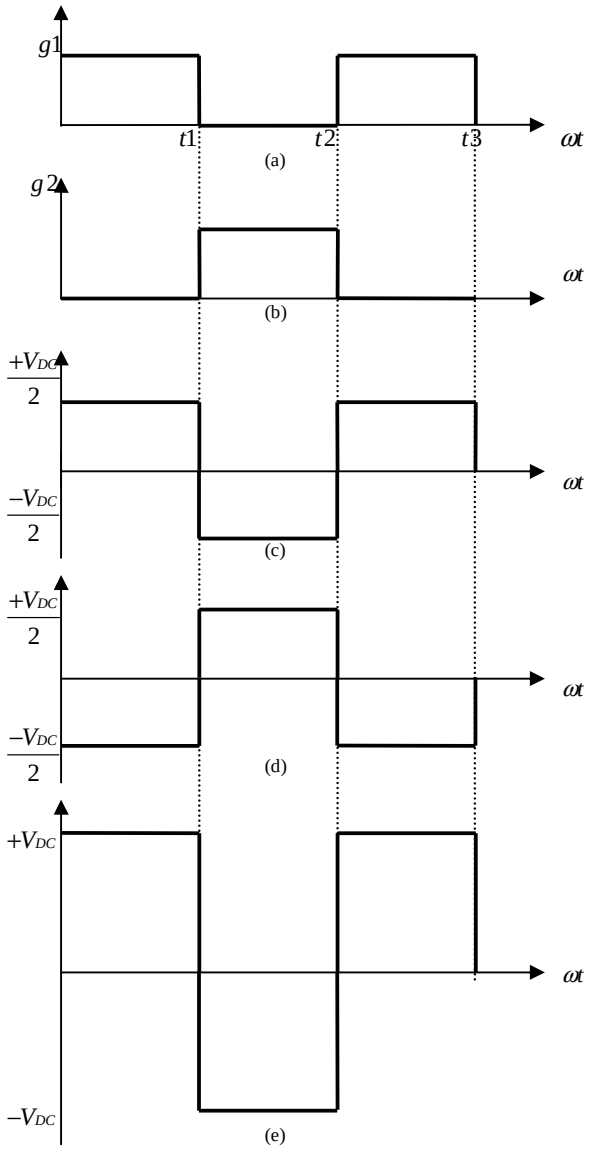

Figure 2.6: Square wave inverters; (a), (b) switching signals, (c) V_{AN} , (d) V_{BN} , (e) v_o

Within the square wave inverters operation, each inverter switch changes its state only twice per cycle. This is important at very high power levels where the solid state switches generally have slower turn on and turn off speeds. However, square wave

switching produces fixed inverter output voltage. Therefore in order to regulate the magnitude of the output voltage, the dc input voltage, V_{DC} to the inverter may be adjusted.