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12. Manual of UP3-1C6 Education Kit, Cyclone Edition

13. Data Sheet DM74LS244

APPENDICES

APPENDIX (A)

VHDL Programming

```
---ma=0.6, mf=21
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY PWM IS
PORT
(
CLOCK_25MHZ:IN STD_LOGIC;
---CLOCK_1M,CLOCK_100K: OUT STD_LOGIC;
---COUNT1:OUT STD_LOGIC_VECTOR (7 DOWNTO 0);--MAIN COUNTER 1 TO 6
---STATE:OUT STD_LOGIC_VECTOR (11 DOWNTO 0);--OUT INTEGER RANGE 1 TO 36

CLOCK_1,CLOCK_2:OUT STD_LOGIC);
END PWM;

ARCHITECTURE A OF PWM IS
SIGNAL COUNT_100KHZ: STD_LOGIC_VECTOR(2 DOWNTO 0);
SIGNAL COUNT_1MHZ: STD_LOGIC_VECTOR(4 DOWNTO 0);
SIGNAL CLOCK_1MHZ_INT, CLOCK_100KHZ_INT: STD_LOGIC;

SIGNAL CYCLE1,CYCLE2: STD_LOGIC_VECTOR(7 DOWNTO 0);
SIGNAL COUNT_1,COUNT_2:STD_LOGIC_VECTOR(7 DOWNTO 0);
SIGNAL COUNT:STD_LOGIC_VECTOR(11 DOWNTO 0); ---INTEGER RANGE 1 TO 36
---MMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMM
SIGNAL CLOCK_1_INT,CLOCK_2_INT:STD_LOGIC;
SIGNAL
DATA1,DATA2,DATA3,DATA4,DATA5,DATA6,DATA7,DATA8,DATA9,DATA10:STD_LOGIC_V
ECTOR(11 DOWNTO 0);
SIGNAL
DATA11,DATA12,DATA13,DATA14,DATA15,DATA16,DATA17,DATA18,DATA19,DATA20:STD
_LOGIC_VECTOR(11 DOWNTO 0);
SIGNAL
DATA21,DATA22,DATA23,DATA24,DATA25,DATA26,DATA27,DATA28,DATA29,DATA30:STD
_LOGIC_VECTOR(11 DOWNTO 0);
SIGNAL
DATA31,DATA32,DATA33,DATA34,DATA35,DATA36,DATA37,DATA38,DATA39,DATA40:STD
_LOGIC_VECTOR(11 DOWNTO 0);
SIGNAL
DU1,DU2,DU3,DU4,DU5,DU6,DU7,DU8,DU9,DU10,DU11,DU12,DU13,DU14,DU15:STD_LOGIC_V
ECTOR(7 DOWNTO 0);
```

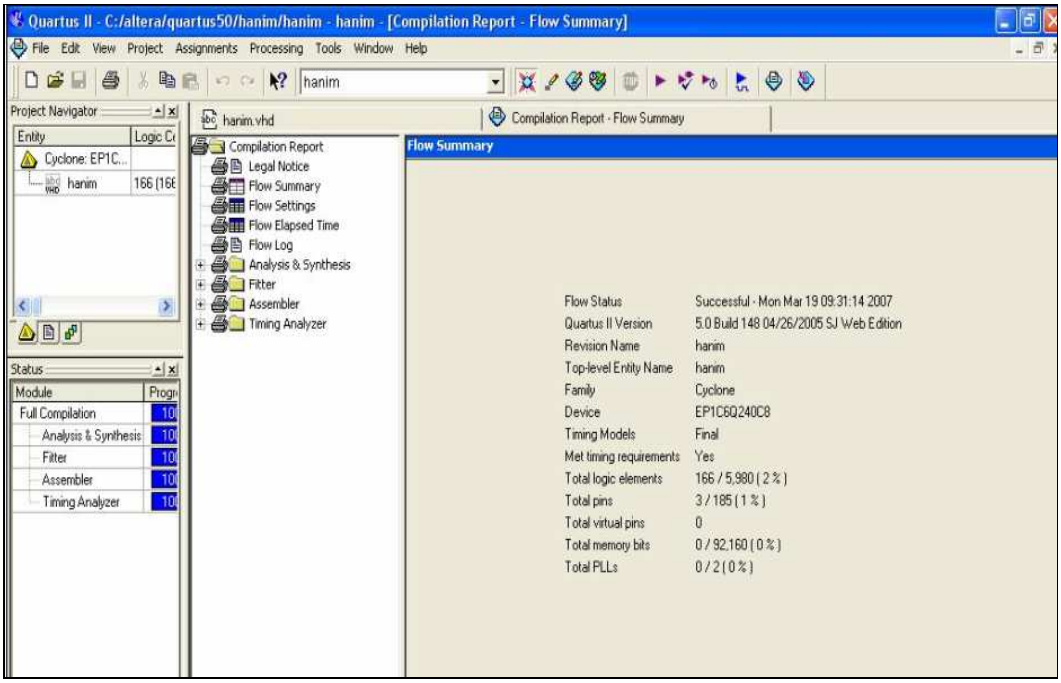
```
SIGNAL
DU16,DU17,DU18,DU19,DU20,DU21,DU22,DU23,DU24,DU25,DU26,DU27,DU28:STD_LOGIC_VE
CTOR(7 DOWNTO 0);
SIGNAL
DU29,DU30,DU31,DU32,DU33,DU34,DU35,DU36,DU37,DU38,DU39,DU40:STD_LOGIC_VECTOR
(7 DOWNTO 0);

BEGIN
-------------------------------------------------------------------------------------------------------
DATA1<=X"032";                  DU1<=X"06";
DATA2<=X"064";                  DU2<=X"09";
DATA3<=X"096";                  DU3<=X"0E";
DATA4<=X"0C8";                  DU4<=X"12";
DATA5<=X"0FA";                  DU5<=X"15";
DATA6<=X"12C";                  DU6<=X"19";
DATA7<=X"15E";                  DU7<=X"1B";
DATA8<=X"190";                  DU8<=X"1D";
DATA9<=X"1C2";                  DU9<=X"1E";
DATA10<=X"1F4";                 DU10<=X"1E";
DATA11<=X"226";                 DU11<=X"1E";
DATA12<=X"258";                 DU12<=X"1D";
DATA13<=X"28A";                 DU13<=X"1B";
DATA14<=X"2BC";                 DU14<=X"19";
DATA15<=X"2EE";                 DU15<=X"15";
DATA16<=X"320";                 DU16<=X"12";
DATA17<=X"352";                 DU17<=X"0E";
DATA18<=X"384";                 DU18<=X"09";
DATA19<=X"3B6";                 DU19<=X"06";
DATA20<=X"3E8";                 DU20<=X"00";
-------------------------------------------------------------------------------------------------------
DATA21<=X"41A";                 DU21<=X"06";
DATA22<=X"44C";                 DU22<=X"09";
DATA23<=X"47E";                 DU23<=X"0E";
DATA24<=X"4B0";                 DU24<=X"12";
DATA25<=X"4E2";                 DU25<=X"15";
DATA26<=X"514";                 DU26<=X"19";
DATA27<=X"546";                 DU27<=X"1B";
DATA28<=X"578";                 DU28<=X"1D";
DATA29<=X"5AA";                 DU29<=X"1E";
DATA30<=X"5DC";                 DU30<=X"1E";
DATA31<=X"60E";                 DU31<=X"1E";
DATA32<=X"640";                 DU32<=X"1D";
DATA33<=X"672";                 DU33<=X"1B";
DATA34<=X"6A4";                 DU34<=X"19";
DATA35<=X"6D6";                 DU35<=X"15";
DATA36<=X"708";                 DU36<=X"12";
DATA37<=X"73A";                 DU37<=X"0E";
DATA38<=X"76C";                 DU38<=X"09";
DATA39<=X"79E";                 DU39<=X"06";
DATA40<=X"7D0";                 DU40<=X"00";
--DATA41<=X"802";               DU41<=X"";
--CLOCK_1M<=CLOCK_1MHZ_INT;
--CLOCK_100K<=CLOCK_100KHZ_INT;

PROCESS
BEGIN
WAIT UNTIL CLOCK_25MHZ'EVENT AND CLOCK_25MHZ='1';
IF COUNT_1MHZ < 47 THEN
COUNT_1MHZ <= COUNT_1MHZ+1;
ELSE
```

```
COUNT_1MHZ <= "00000";
END IF;
IF COUNT_1MHZ <24 THEN
CLOCK_1MHZ_INT <= '0';
ELSE
CLOCK_1MHZ_INT <= '1';
END IF;
END PROCESS;

PROCESS
BEGIN
WAIT UNTIL CLOCK_1MHZ_INT'EVENT AND CLOCK_1MHZ_INT='1';
IF COUNT_100KHZ /= 4 THEN
 COUNT_100KHZ<= COUNT_100KHZ+1;
ELSE
COUNT_100KHZ<="000";
CLOCK_100KHZ_INT<= NOT CLOCK_100KHZ_INT;
END IF;
END PROCESS;

PROCESS
BEGIN
--WAIT UNTIL CLOCK_100KHZ_INT'EVENT AND CLOCK_100KHZ_INT='1';

WAIT UNTIL CLOCK_25MHZ'EVENT AND CLOCK_25MHZ='1';
IF COUNT <2000 THEN ----SAMPLE 10 CYCLE PER CHANNEL
COUNT<= COUNT+1;
ELSE
COUNT<="000000000001";
END IF;
-------STATE<=COUNT;

IF COUNT=DATA40 OR COUNT<DATA1 THEN  ---00--10
          CYCLE1<=DU1; CYCLE2<="00000000";---1
ELSIF COUNT >= DATA1 AND COUNT < DATA2 THEN ---10--20
          CYCLE1<=DU2; CYCLE2<="00000000";---2
ELSIF COUNT >= DATA2 AND COUNT<DATA3 THEN--20--30
          CYCLE1<=DU3; CYCLE2<="00000000";---3
ELSIF COUNT >= DATA3 AND COUNT<DATA4 THEN--20--30
          CYCLE1<=DU4; CYCLE2<="00000000";---4
ELSIF COUNT >= DATA4 AND COUNT<DATA5 THEN--10--20
          CYCLE1<=DU5; CYCLE2<="00000000";---3
ELSIF COUNT >= DATA5 AND COUNT<DATA6 THEN--20--30
          CYCLE1<=DU6; CYCLE2<="00000000";---2
ELSIF COUNT >= DATA6 AND COUNT<DATA7 THEN--10--20
          CYCLE1<=DU7; CYCLE2<="00000000";---1
ELSIF COUNT >= DATA7 AND COUNT<DATA8 THEN--00--10
          CYCLE1<=DU8; CYCLE2<="00000000";---1
ELSIF COUNT >= DATA8 AND COUNT<DATA9 THEN--10--20
          CYCLE1<=DU9; CYCLE2<="00000000";---2
ELSIF COUNT >= DATA9 AND COUNT<DATA10 THEN--20--30
          CYCLE1<=DU10; CYCLE2<="00000000";---3
-------------------------------------------------------------------------------------------------------------------
ELSIF COUNT >= DATA10 AND COUNT<DATA11 THEN
          CYCLE1<=DU11; CYCLE2<="00000000";---4
-------------------------------------------------------------------------------------------------------------------
ELSIF COUNT >= DATA11 AND COUNT<DATA12 THEN--10--20
          CYCLE1<=DU12; CYCLE2<="00000000";---3
ELSIF COUNT >= DATA12 AND COUNT<DATA13 THEN--20--30
          CYCLE1<=DU13; CYCLE2<="00000000";---3
```

```
ELSIF COUNT >= DATA13 AND COUNT<DATA14 THEN--10--20
        CYCLE1<=DU14; CYCLE2<="00000000";---2
ELSIF COUNT >= DATA14 AND COUNT<DATA15 THEN--00--10
        CYCLE1<=DU15; CYCLE2<="00000000";---1
ELSIF COUNT >= DATA15 AND COUNT<DATA16 THEN--10--20
        CYCLE1<=DU16; CYCLE2<="00000000";---1
ELSIF COUNT >= DATA16 AND COUNT<DATA17 THEN--20--30
        CYCLE1<=DU17; CYCLE2<="00000000";---2
ELSIF COUNT >= DATA17 AND COUNT<DATA18 THEN--10--20
        CYCLE1<=DU18; CYCLE2<="00000000";---3
ELSIF COUNT >= DATA18 AND COUNT<DATA19 THEN--20--30
        CYCLE1<=DU19; CYCLE2<="00000000";---4
ELSIF COUNT >= DATA19 AND COUNT<DATA20 THEN--20--30
        CYCLE1<=DU20; CYCLE2<="00000000";---3
----------"---------"----------
ELSIF COUNT >= DATA20 AND COUNT<DATA21 THEN--10--20
        CYCLE2<=DU21; CYCLE1<="00000000";---2
ELSIF COUNT >= DATA21 AND COUNT<DATA22 THEN--00--10
        CYCLE2<=DU22; CYCLE1<="00000000";---1
ELSIF COUNT >= DATA22 AND COUNT<DATA23 THEN--10--20
        CYCLE2<=DU23; CYCLE1<="00000000";---2
ELSIF COUNT >= DATA23 AND COUNT<DATA24 THEN--20--30
        CYCLE2<=DU24; CYCLE1<="00000000";---3
ELSIF COUNT >= DATA24 AND COUNT<DATA25 THEN--20--30
        CYCLE2<=DU25; CYCLE1<="00000000";---4
ELSIF COUNT >= DATA25 AND COUNT<DATA26 THEN--10--20
        CYCLE2<=DU26; CYCLE1<="00000000";---3
ELSIF COUNT >= DATA26 AND COUNT<DATA27 THEN--20--30
        CYCLE2<=DU27; CYCLE1<="00000000";---2
ELSIF COUNT >= DATA27 AND COUNT<DATA28 THEN--10--20
        CYCLE2<=DU28; CYCLE1<="00000000";---1
ELSIF COUNT >= DATA28 AND COUNT<DATA29 THEN--00--10
        CYCLE2<=DU29; CYCLE1<="00000000";---1
ELSIF COUNT >= DATA29 AND COUNT<DATA30 THEN--10--20
        CYCLE2<=DU30; CYCLE1<="00000000";---2
ELSIF COUNT >= DATA30 AND COUNT<DATA31 THEN--20--30
        CYCLE2<=DU31; CYCLE1<="00000000";---3
----------
ELSIF COUNT >= DATA31 AND COUNT<DATA32 THEN--20--30
        CYCLE2<=DU32; CYCLE1<="00000000";---4
----------
ELSIF COUNT >= DATA32 AND COUNT<DATA33 THEN--10--20
        CYCLE2<=DU33; CYCLE1<="00000000";---3
ELSIF COUNT >= DATA33 AND COUNT<DATA34 THEN--20--30
        CYCLE2<=DU34; CYCLE1<="00000000";---3
ELSIF COUNT >= DATA34 AND COUNT<DATA35 THEN--10--20
        CYCLE2<=DU35; CYCLE1<="00000000";---2
ELSIF COUNT >= DATA35 AND COUNT<DATA36 THEN--00--10
        CYCLE2<=DU36; CYCLE1<="00000000";---1
ELSIF COUNT >= DATA36 AND COUNT<DATA37 THEN--10--20
        CYCLE2<=DU37; CYCLE1<="00000000";---1
ELSIF COUNT >= DATA37 AND COUNT<DATA38 THEN--20--30
        CYCLE2<=DU38; CYCLE1<="00000000";---2
ELSIF COUNT >= DATA38 AND COUNT<DATA39 THEN--10--20
        CYCLE2<=DU39; CYCLE1<="00000000";---3
ELSIF COUNT >= DATA39 AND COUNT<DATA40 THEN--20--30
        CYCLE2<=DU40; CYCLE1<="00000000";---4

        END IF;
        END PROCESS;
```

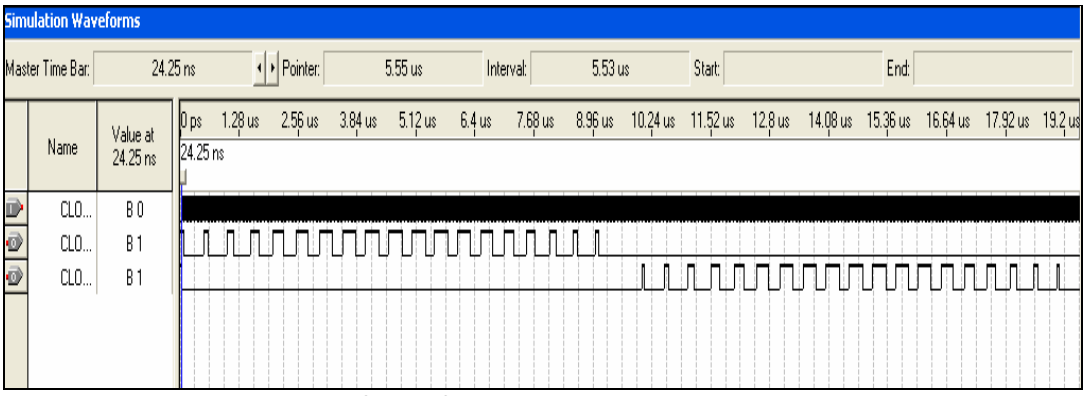
```
-------------------------------------------------------------------------------------------------------------
PROCESS
BEGIN
----WAIT UNTIL CLOCK_100KHZ_INT'EVENT AND CLOCK_100KHZ_INT='1';
WAIT UNTIL CLOCK_25MHZ'EVENT AND CLOCK_25MHZ='1';

-------------------------------------------------------------------------------------------------------------
IF COUNT_1<50 THEN
COUNT_1<=COUNT_1+1;
ELSE
COUNT_1<="00000001";
END IF;
--COUNT1<=COUNT_1;---TRACE OUTPUT

-----------------C1-------------------------------------------------------
IF COUNT_1<= CYCLE1 THEN
CLOCK_1_INT<='1';
ELSE
CLOCK_1_INT<='0';
END IF;
CLOCK_1<=CLOCK_1_INT;---------OUTPUT

----------------------C2-----------------------------------------------------------

IF COUNT_1 <=CYCLE2 THEN
CLOCK_2_INT<='1';
ELSE
CLOCK_2_INT<='0';
END IF;
CLOCK_2<=CLOCK_2_INT;---OUTPUT
END PROCESS;
END A;
```

APPENDIX A (i)



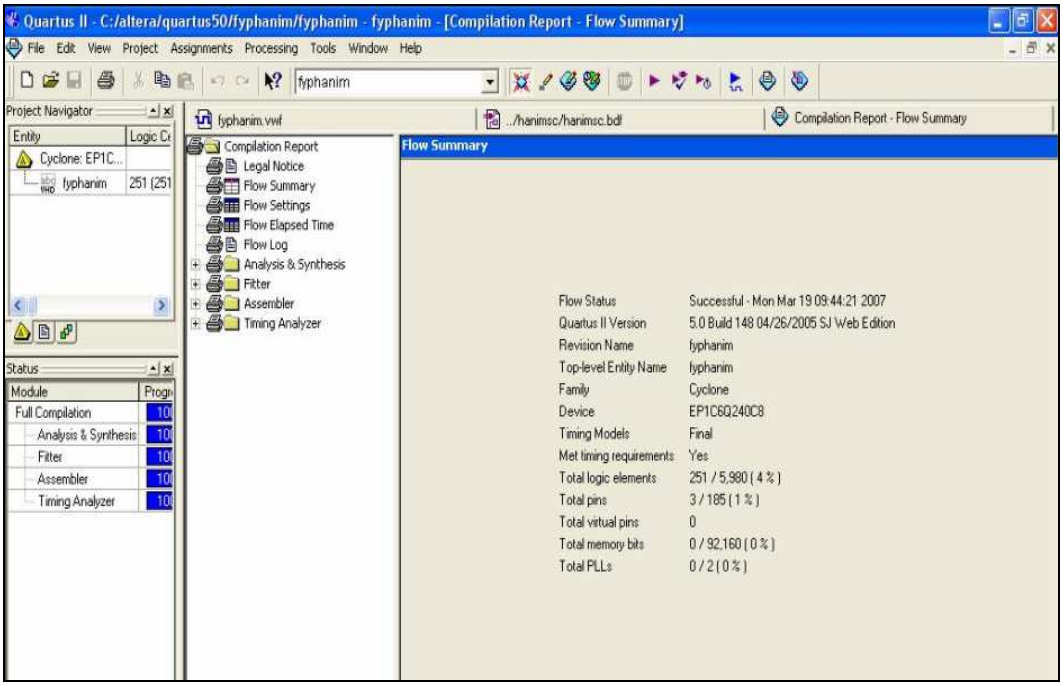
Flow summary after done the compilation of VHDL Programming

APPENDIX A (ii)



Simulation waveform after completed the VHDL Programming

APPENDIX A (iii)



Flow summary after done the compilation of Block Diagram

FAIRCHILD SEMICONDUCTOR TM

August 1986
Revised March 2000

DM74LS244
Octal 3-STATE Buffer/Line Driver/Line Receiver

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

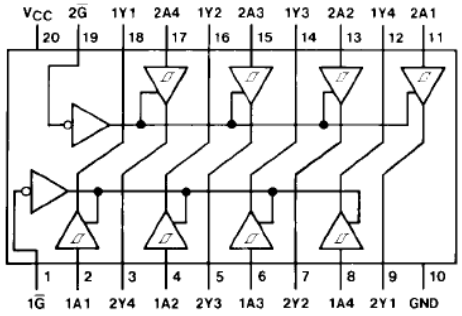
- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current) 24 mA
- Typical I_{OH} (source current) −15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = LOW Logic Level
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min		0.2	0.4		V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	LOW Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA			0.4	V
			I_{OL} = Max			0.5	
I_{OZH}	Off-State Output Current, HIGH Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V			20	µA
I_{OZL}	Off-State Output Current, LOW Level Voltage Applied		V_O = 0.4V			−20	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max	V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max	V_I = 0.4V	−0.5		−200	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs HIGH		13	23	mA
			Outputs LOW		27	46	
			Outputs Disabled		32	54	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

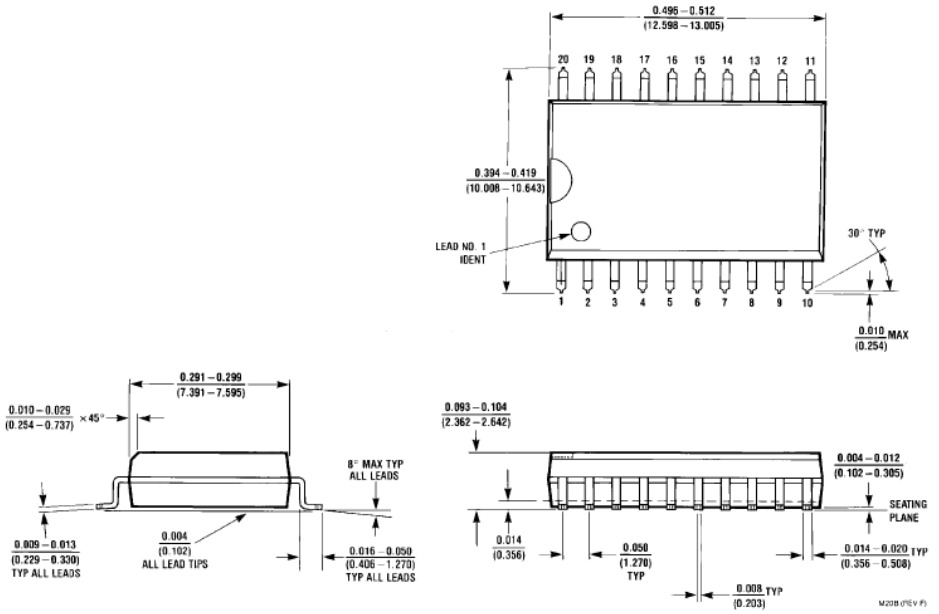
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V, T_A = 25°C

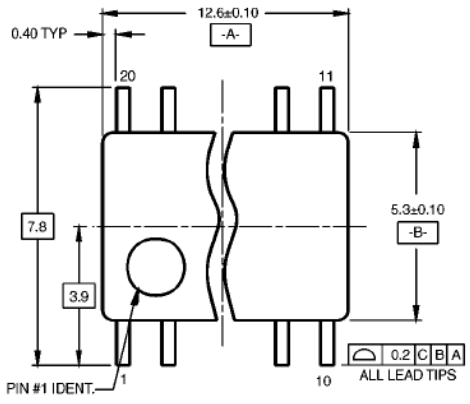
Symbol	Parameter	Conditions	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 45 pF R_L = 667Ω	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	C_L = 45 pF R_L = 667Ω	18	ns
t_{PZL}	Output Enable Time to LOW Level	C_L = 45 pF R_L = 667Ω	30	ns
t_{PZH}	Output Enable Time to HIGH Level	C_L = 45 pF R_L = 667Ω	23	ns
t_{PLZ}	Output Disable Time from LOW Level	C_L = 5 pF R_L = 667Ω	25	ns
t_{PHZ}	Output Disable Time from HIGH Level	C_L = 5 pF R_L = 667Ω	18	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 150 pF R_L = 667Ω	21	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	C_L = 150 pF R_L = 667Ω	22	ns
t_{PZL}	Output Enable Time to LOW Level	C_L = 150 pF R_L = 667Ω	33	ns
t_{PZH}	Output Enable Time to HIGH Level	C_L = 150 pF R_L = 667Ω	26	ns

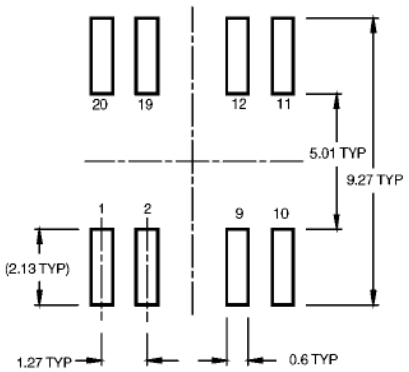
Physical Dimensions inches (millimeters) unless otherwise noted



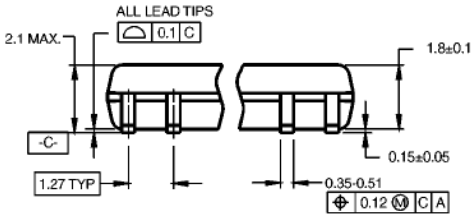
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

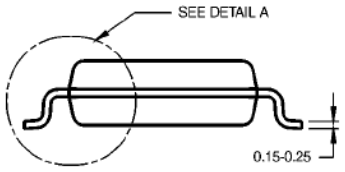


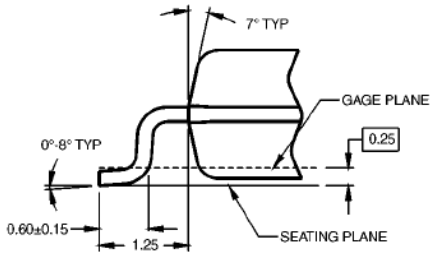


LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS





DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

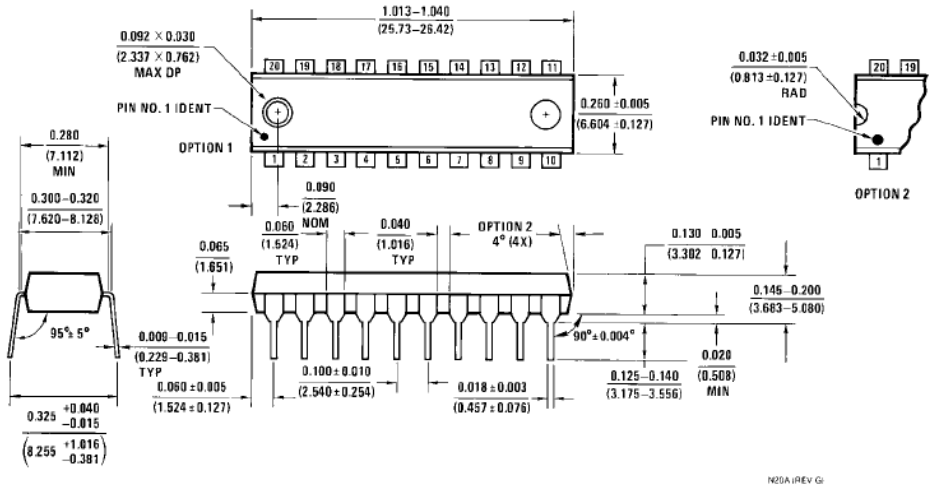
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



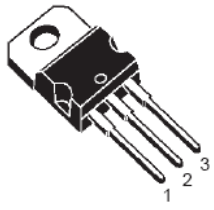
20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

IRF840

N - CHANNEL 500V - 0.75Ω - 8A - TO-220
PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF840	500 V	< 0.85 Ω	8 A

- TYPICAL $R_{DS(on)}$ = 0.75 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-220

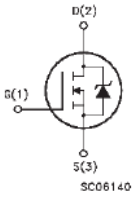
DESCRIPTION

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVER

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	500	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	8.0	A
I_D	Drain Current (continuous) at T_c = 100 °C	5.1	A
I_{DM}(•)	Drain Current (pulsed)	32	A
P_{tot}	Total Dissipation at T_c = 25 °C	125	W
	Derating Factor	1.0	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area (1) $I_{SD} \le 8A$, $di/dt \le 100$ A/µs, $V_{DD} \le V_{(BR)DSS}$, $Tj \le T_{JMAX}$
First Digit of the Datecode Being Z or K Identifies Silicon Characterized in this Datasheet

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.0	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	oC/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	8.0	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	520	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 4.8 A		0.75	0.85	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	8.0			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 4.8 A	4.9			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1300 200 18		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 250 V I_D = 4.3 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		19 11		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400 V I_D = 8.0 A V_{GS} = 10 V		39 10.6 13.7	50	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 400 V I_D = 8 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		11.5 11 20		ns ns ns

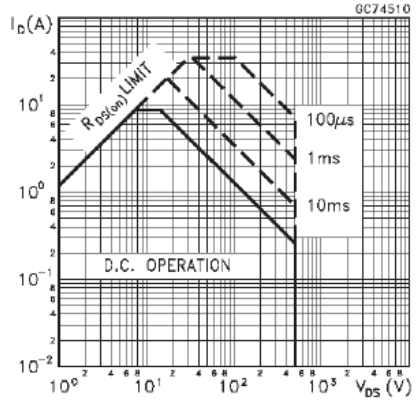
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				8.0 32	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 8.0 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 8.0 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 5)		420 3.5 16.5		ns µC A

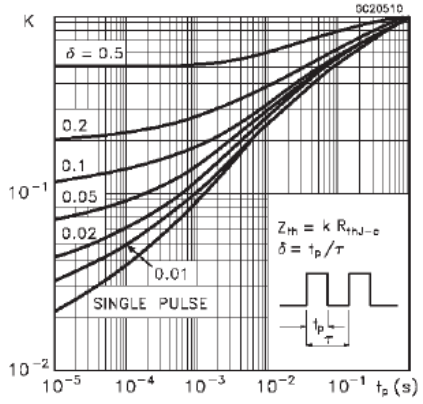
(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

(•) Pulse width limited by safe operating area

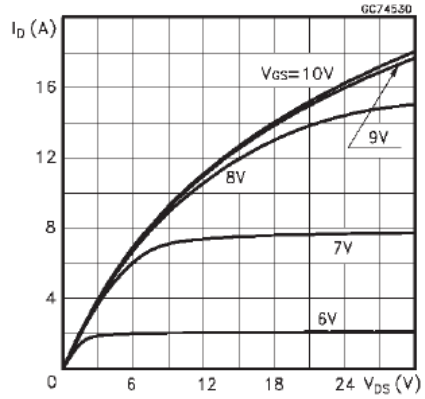
Safe Operating Area



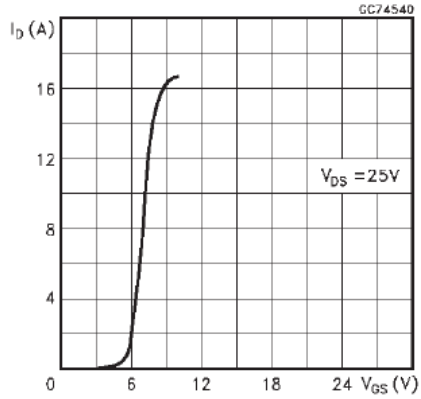
Thermal Impedance



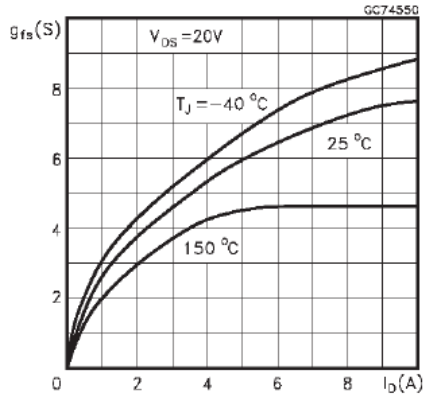
Output Characteristics



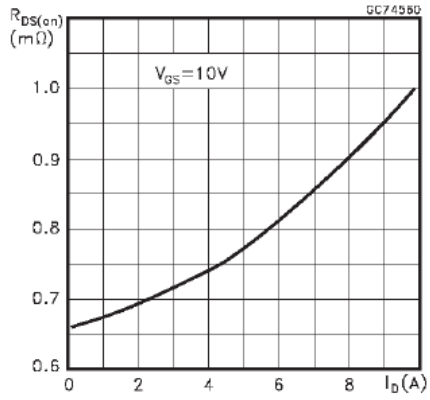
Transfer Characteristics



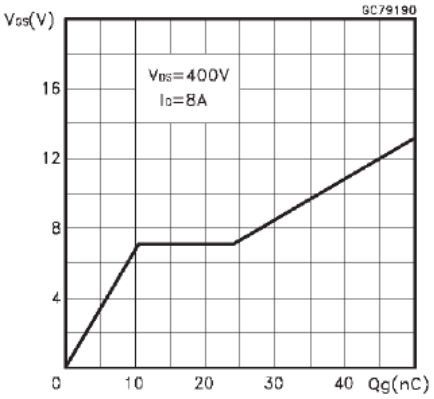
Transconductance



Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage



Capacitance Variations

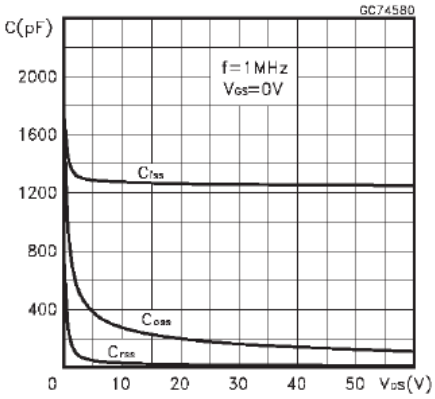


Fig. 1: Unclamped Inductive Load Test Circuit

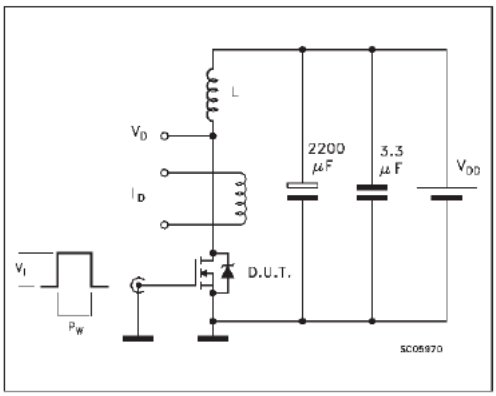


Fig. 1: Unclamped Inductive Waveform

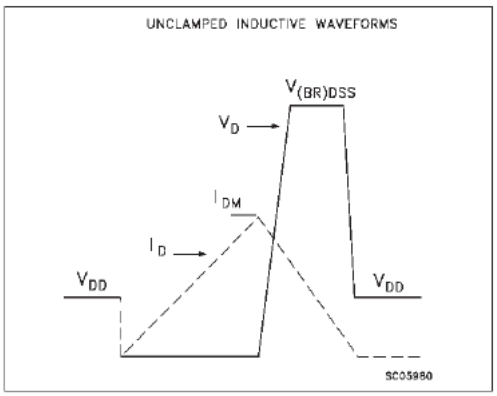


Fig. 3: Switching Times Test Circuits For Resistive Load

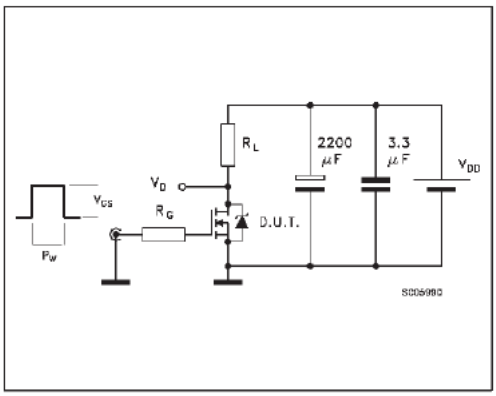


Fig. 4: Gate Charge test Circuit

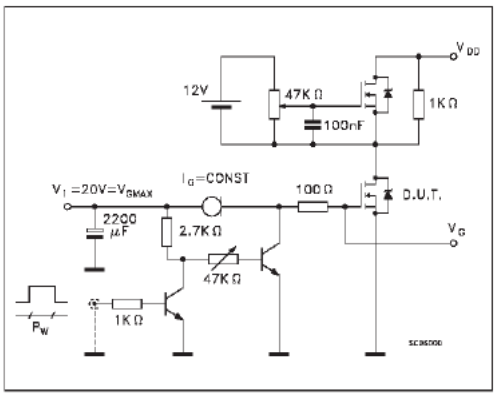
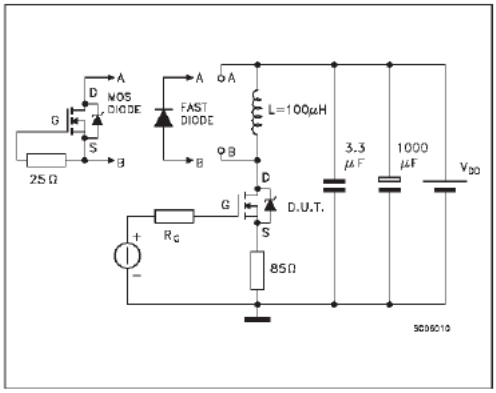


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151