CHAPTER 5

CONCLUSION

5.0 Summary

As a summary, chapter 1 has simply briefed about the objective, scope of study, theories involved and background research. Chapter 1 also has discussed about the semiconductor device technology such as ion implantation and diffusion process which are important in the fabrication of CMOS and bipolar transistor.

Chapter 2 has discussed on all of the theories involved in the project. The theories involved such as ion implantation technology, diffusion process, point defect mechanisms (interstitial, vacancy and cluster) and transient enhanced diffusion. This chapter also includes all the equations and figures that related to the theories.

Chapter 3 explained about the methodology involved in generating structures in the process simulation, basically this chapter is focused on the step by step process from structure generation to the analyzation. All the steps are clearly showed in the figures. Further more, parameters and the coefficient value used in the simulation are also stated in the table. The descriptions of the step-by-step methodology are stated based on the command, parameter and statement.

Chapter 4 discussed about the results obtained from the process simulation using Taurus TSUPREM 4. The Analyzation is done by observing the graphs that are generated

form the data that were collected from the simulation. The role of boron concentration, interstitials, vacancies, clusters and evolution of diffusion based on different time of annealing for boron diffusion in silicon are discussed.

In conclusion, a study has been done to investigate the effect of a BF_2^+ implant on boron diffusion in silicon. In the simulation, the BF_2^+ not only suppressed boron transient enhanced diffusion but also significantly reduce the boron thermal diffusion. Then, from the experiment, it is proposed that the presence of the fluorine in BF_2^+ can act as sink for interstitial boron and consequently, reduced the boron diffusion in order to obtain a good prediction before a realistic fabrication can be done.

From the result that had been show in chapter 4, the sample implanted high concentration BF_2^+ more reduce the transient enhanced diffusion compared the low concentration of BF_2^+ implant. Further more, the time, dose and energy are important parameter in correlate the boron transient enhanced diffusion.

From the result of these experiment and the computer simulation, it is believe that the project have consist physical picture of the way fluorine implant and interstitial are produced and interact with boron to produce the TED. The shape of the boron profile changed with changes in the ratio of the fluorine energy. The simulations well reproduce the experimental profile. Therefore, the model for TED improved and presented in this study could be considered as qualitatively satisfactory.

5.1 Recommendation for future project

The transient enhanced diffusion (TED) of ion implanted boron in silicon is a major problem in the fabrication of the CMOS and bipolar junction transistor for advanced integrated circuits. The transient enhanced diffusion of dopants in silicon is a central issue in silicon device processing. It is because TED is a limiting factor for shallow junction formation. It is important to understanding and quantifying the phenomenon of transient enhanced diffusion of dopants as one of the central challenges in ion implantation research and development.

As the device size shrinks to be smaller in the future, it becomes more important to understand and have further research and development to reduce the boron transient enhanced diffusion and boron thermal diffusion.

The first recommendation to reduce the transient enhanced diffusion is by the investigation on higher fluorine implantation energies using numerical simulation. By using the higher implantation energies, the trend on transient enhanced diffusion and boron thermal diffusion will be observed

The second recommendation is by the investigation on the dose, time and annealing temperature on the boron transient enhanced diffusion and thermal diffusion. By doing this project, the recipe of the optimum rate to reduce transient enhanced diffusion can be observed.

The third recommendation is by reducing the boron diffusion using the carbon doped in the underlying layer. This method is found able to reduce the diffusion of boron in order to get ultra-shallow junction. The further investigation and research can be done to improve the result.

5.2 Commercialization potential

As higher gate densities and higher frequencies are required for silicon integrated circuits, smaller device dimensions, both laterally and in depth are required. Manufacturing of shallow PN junctions, using boron implantation, presents many difficulties. This is due to the large range of projection for boron, the high diffusivity and the transient enhanced diffusion of boron implanted in silicon [17]. In order to produce very large scale integrated transistor, boron must be implanted into silicon to create high resolution ultra-shallow junction structure. The implantation of boron and other ion in the CMOS process flow creates damage in the silicon lattice the enhanced the interstitial diffusion mechanisms of boron. To control the diffusion of boron it is than necessary to interact with these enhanced interstitial mechanisms. Equally importance is that boron must remain in solution with the silicon lattice and be electrically active to be useful in CMOS [26].

The implantation of BF2+ molecular ions into silicon has been reported to have advantages of higher electrical activation and lower leakage current for PN junctions compared with boron implantation. In addition, the energy partition for the boron ion in the BF2+implantation is on 22% [17]. In integrated circuit chip manufacturing, many ion implantation processes are involved to make the millions of tiny, functional transistor on the silicon wafer surface. Because of the different requirement of dopant concentration and junction depth, the ion implantation energy and ion beam current for these implantation process are quite different. In and advanced semiconductor fabrication room, different kinds of implanter are employed to meet these required. A silicon wafer needs to be doped to change its conductivity in designated areas to form junctions, such as wells and source/drain for CMOS integrated circuits. For the bipolar integrated circuit, doped junctions are needed to form the buried layer, emitter, collector and base [3].

These researches give the advantage for the semiconductor company to improve their devices performance and quality. The reduction of boron diffusion in silicon permit the realization of shallow junction in bipolar junction transistor and CMOS transistors would benefit the fabrication of high performance devices.

With the knowledge in the reducing boron diffusion by fluorine implantation, the interest semiconductor company will need the consultancy services from expertise. With the services that provided to the company, it will be a good business potential. By providing the knowledge and service to the company, the interest company will pay amount of sufficient money for the services.

Further more, the knowledge and the theories about the ion implantation and reduction in boron diffusion by implantation also can be publish. The books that publish can be selling to the student for their studies and research. The company can buy the books as references to make their own recipe to improve their device by reducing the boron diffusion for their device. It is good commercialization potential plan.

Next, if some semiconductor company has interest about the researches in ion implantation reducing the boron diffusion, the company will invited and give a good pay salary and fund to precede the research project.

Conclusion, this research can make a good business plan and also have a good commercialization potential in the future.