HIGH SPEED SIX OPERANDS 16-BITS CARRY SAVE ADDER

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by

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Report submitted in partial fulfillment
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APPROVAL AND DECLARATION SHEET

This project report titled High-Speed Six Operands 16-bits Carry Save Adder was prepared and submitted by Awatif Binti Hashim (Matrix Number: 031030048) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in Universiti Malaysia Perlis (UniMAP).

Checked and Approved by

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Enam Penambahan bagi 16-bit Pembawa Penyimpan Penambah (CSA) Berkelajuan Tinggi

ABSTRAK

Penambah banyak dijumpai dalam gabungan blok-blok mikroproses dan juga cip digital isyarat proses. Kajian yang lepas menyatakan penyebaran yang lambat dan saiz adalah faktor penting dalam menentukan kualiti sesuatu penambah. Tujuan projek ini dibuat adalah untuk implimentasi 3 tahap/peringkat 6 operasi penambah bagi 16-bit Pembawa Penyimpan Penambah CSA dengan Pembawa Riak Penambah (RCA) pada akhir rekaan litar. Objektif projek ini adalah untuk merekacipta pelaksanaan lebih cepat bagi CSA dengan menggunakan rekaan get-get logik dan implimentasikannya pada litar Altera UP2. Projek ini disimulasi dan hasilnya dapat dilihat dengan jelas menggunakan perisian Quartus II dan litar Altera UP2 untuk mengesahkan senibina rekabentuk. Litar yang berkelajuan tinggi telah direka dengan cara mencari kelambatan yg paling sedikit antara lima jenis litar Full Adder(FA) dan juga dengan cara menambah litar yang mempengaruhi kelajuan. Projek ini telah mencapai kelajuan dari 16.84MHz ke 90.09MHz laju dengan menggunakan peranti EPF10K70RC240-4. Keputusan menyumbangkan rekabentuk CSA yang lebih laju.

ABSTRACT

Adders are commonly found in the critical path of many building blocks of microprocessors and digital signal processing chips. The most important for measuring the quality of adder designs in the past were propagation delay, and area. The purpose of the project is to implement a high-speed three levels six operands of 16-bits CSA with RCA at the end of the design. The objective of this project are design faster execution of CSA using gate logic design and implement it to the Altera UP2 board. The project is simulated and clarifies the output using Quartus II software and Altera UP2 board implementation to verify the design architectures. The high-speed circuit was designed by using smallest delay between five different logic gates Full Adder (FA) and by adding pipeline. This project has been achieved from 16.84MHz to the 90.09MHz speed on EPF10K70RC240-4 device. This result contribute CSA is in faster speed.

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