

## REFERENCES

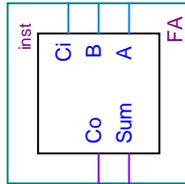
- [1] Behrooz Parhami, (2000). *Computer Arithmetic : Algorithm and hardware design*, 2<sup>nd</sup> Edition, Oxford University Press, New York.
- [2] Prof. Loh, (1996) *Carry-Save Addition Processor Design*, The University of Texas, Austin.
- [3] Israel Koren, (2001). *Computer Arithmetic Algorithms: Fast Addition*, 2<sup>nd</sup> Edition, University of Massachusetts, Canada.
- [4] Naofumi Takagi, Haruyuki Tago, Baugh C. R. and Saburo Muroga, (2003). *Logic Design : Adders*
- [5] Earl E. Swartzlander, Jr., (2002). *Computer Arithmetic : High speed computer arithmetic*, the computer engineering handbook, CRC Press, LLC.
- [6] Tyc, (2000). *Multioperand Adder*, Dept. of Electrical Engineering, National Tsing Hua University, China.
- [7] .Adnan, (1999). *Multi Addition Adder*, Dept. of Electrical and Computer Engineering, The University of Texas, Austin.
- [8] Oliver Sinnen, (2002). *Reconfigurable Computing : Multipliers*, Dept. of Electrical and Computer Engineering, Michigan State University of Auckland, New Zealand.
- [9] Manzkem, (2002). *Adder : Multiple Addition*, Dept. of Electrical and Computer Engineering Michigan State University College of Engineering, USA.
- [10] Andrew Soh, (1996). *Introduction and Integer Addition*, Computer Science Dept., New Jersey Institute of Technology, USA.
- [11] Prof. Bill Dally, Concurrent VLSI Architecture CVA Group's World Wide Web Home Page, *The Coming Revolution in Computer Architecture*, University of Stanford, USA.

- [12] Dr. Sharad Seth, Yifeng Zhu, (2005). *Combinational Logic Design and Timing*, Computer Organization and Architecture University of Maine, UK.
- [13] Seiji Kajihara and Tsutomu Sasao, (1997). *On the Adders with Minimum Tests*, IEEE Transaction in Department of Computer Science and Electronics, Kyushu Institute of Technology, Japan.
- [14] Prof. Dr.-Ing. Wolfgang Kunz, Technische Universität Kaiserslautern, (2005), *Algorithmic Design of Arithmetic Circuit*, Spain. [www-eda.eit.uni-kl.de](http://www-eda.eit.uni-kl.de).
- [15] Dr. Sharad Seth, Yifeng Zhu, (2005). *Combinational Logic Design and Timing*, Computer Organization and Architecture University of Maine, UK.
- [16] Floyd, (2006), *Digital Fundamentals*, 8<sup>th</sup> Edition, Pearson Prentice Hall.
- [17] Taewhan Kim, William Jao, and Steve Tjiang, (1998). Circuit Optimization Using Carry Save Adder Cells, IEEE Transactions on Computer-Aided Design Of Integrated Circuits and Systems, Vol. 17.
- [18] Anup Hosangadi, Farzan Fallah, Ryan Kastner, (2006). *Optimizing High Speed Arithmetic Circuits Using Three-Term Extraction*, ACM journal.
- [19] Tobias G. Nöl, *Carry-Save Arithmetic for High-speed Digital Signal Processing*, Cambridge University Press, UK.
- [20] Xingcha Fan, Richard G. Burford and Neil W. Bergmann, *Design Technique for High Performance Arithmetic Operators*, Cambridge University Press, UK.
- [21] Oscar Gustafsson, Herzi Olilsoii, and Lars Wanhammar, (2004). Minimum adder integer multipliers using Carry Save Adder, *Proc. IEEE Int. Symp. Circuits Syst.*, Sydney, Australia.
- [22] O. Gustafsson, H. Ohlsson, and L. Wanhammar, (May 2001). Minimum adder integer multipliers using carry-save adders, *Proc. IEEE Int. Symp. Circuits Syst.*, Sydney, Australia, vol. II, pp. 709–712.
- [23] Marcelo Rosa Fonseca, Eduardo A. C. da Costa, Sergio Bampi and José C, (2005). Monteiro Performance Optimization of Radix-2<sup>m</sup> Multipliers Using Carry Save Adders, IEEE, Universidade Católica de Pelotas.
- [24] John Cooley, EDA & ASIC Design Consultant in Synopsys, Verilog, VHDL and numerous Design Methodologies, University of Moratuwa, Sri Lanka Department of Computer Science & Engineering

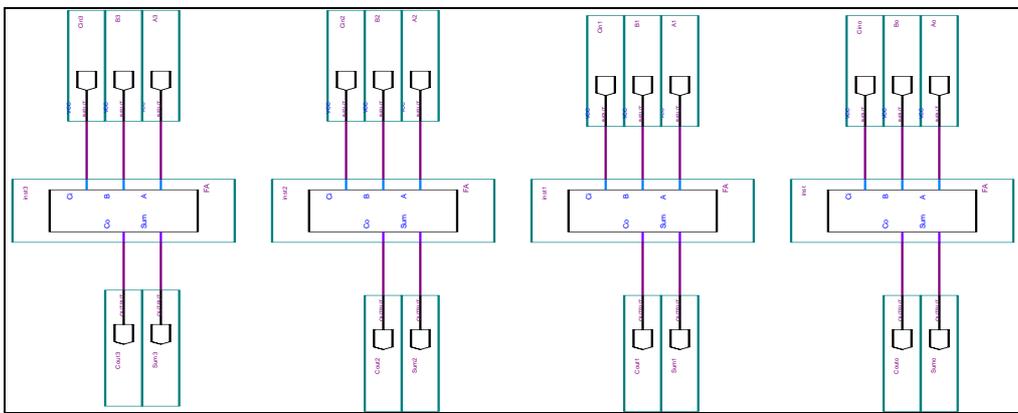
- [25] Phil Gossett, (2000). *Quantum Carry Save Arithmetic*, Cornell University Library, Ithaca, NY.
- [26] Chetana Nagendra, Irwin M. J., Owens R. M., (1996). Area-Time-Power Tradeoffs in Parallel Adders, IEEE Transactions on Circuits and Systems, Vol. 43.
- [27] Prof. Vojin G. Oklobdzija, (1999). *High-Speed VLSI Arithmetic Units: Adders and Multipliers*, School of Computer and Communication Sciences, University of California, USA.
- [28] Mohammed Sayed and Wael Badawy, (2002). Performance Analysis of Single Full Adder Cells Using 0.18, 0.25 and 0.35 $\mu$ m CMOS Technology, IEEE, Transaction on Electrical and Computer Engineering, University of Calgary, Canada.
- [29] Amir Ali Khatibzadeh and Kaamran Raahemifar, (2004). A Study and Comparison of Full Adder Cells Based On The Standard Static CMOS Logic, IEEE, Trans. on Electrical and Computer Engineering.
- [30] T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy, (May 2006). A Novel Low Power, High Speed 14 Transistor CMOS Full Adder Cell with 50% Improvement in Threshold Loss Problem, IEEE Trans. On Engineering, Computing and Technology Volume 13.
- [31] James Levy, Jabulani Nyathi, and Jos´e Delgado-Frias, (2005). High-Performance Parallel Addition Using Hybrid Wave-Pipelining, IEEE Transaction of EECS.
- [32] Altera University Program UP2 Education kit user guide (2004). Vol. 3.1.
- [33] Prof. Dr.-Ing. Wolfgang Kunz, Technische Universitat Kaiserslautern, (2005), *Algorithmic Design of Arithmetic Circuit*, [www-eda.eit.uni-kl.de](http://www-eda.eit.uni-kl.de).
- [34] Synopsys Inc., Design Ware Components Databook, 1996.
- [35] John R, Gregg, (1986), *Ones and Zeros : Understanding Boolean algebra, digital circuits, and the logic of sets*, IEEE Press Understanding Science and Technology Series, New York.
- [36] Floyd, (2006). *Digital Fundamentals*, 9<sup>th</sup> Edition, Pearson Prentice Hall.
- [37] John F Wakerly, (2001), *Digital Design Principal and Practices*, 3<sup>th</sup> editon, Stanford University, New Jersey.

- [38] Earl E. Swartzlander, Jr., (2002). Computer Arithmetic : High speed computer arithmetic, the computer engineering handbook, CRC Press, LLC.
- [39] Single Digit Numeric Display Seven Segment, NTE Electronic inc., Bloomfield
- [40] Amin Ismail and Victor M. Rooney, (2002). *Digital concepts and applications*, 2<sup>nd</sup> edition, Harcout Brace College Publisher.
- [41] Single Digit Numeric Display Seven Segment, NTE Electronic inc., Bloomfield

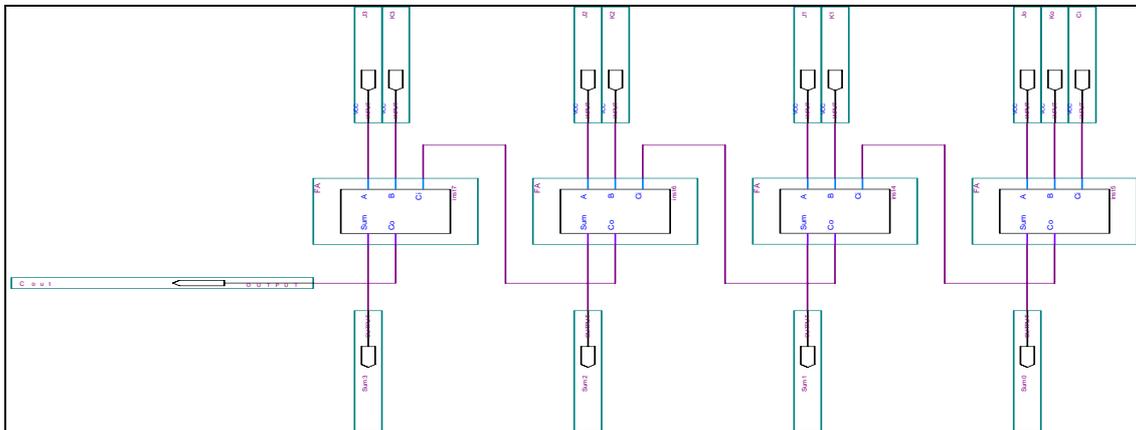
## Appendix A



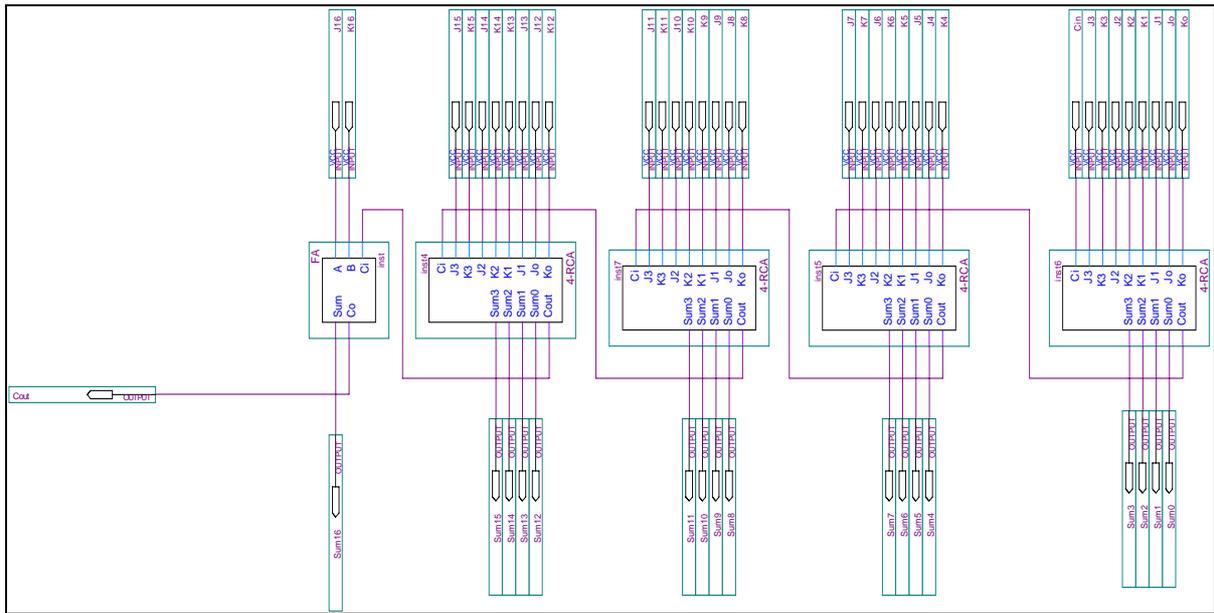
**Appendix A (i) : FA block symbol**



**Appendix A (ii) : 4-bit CSA**

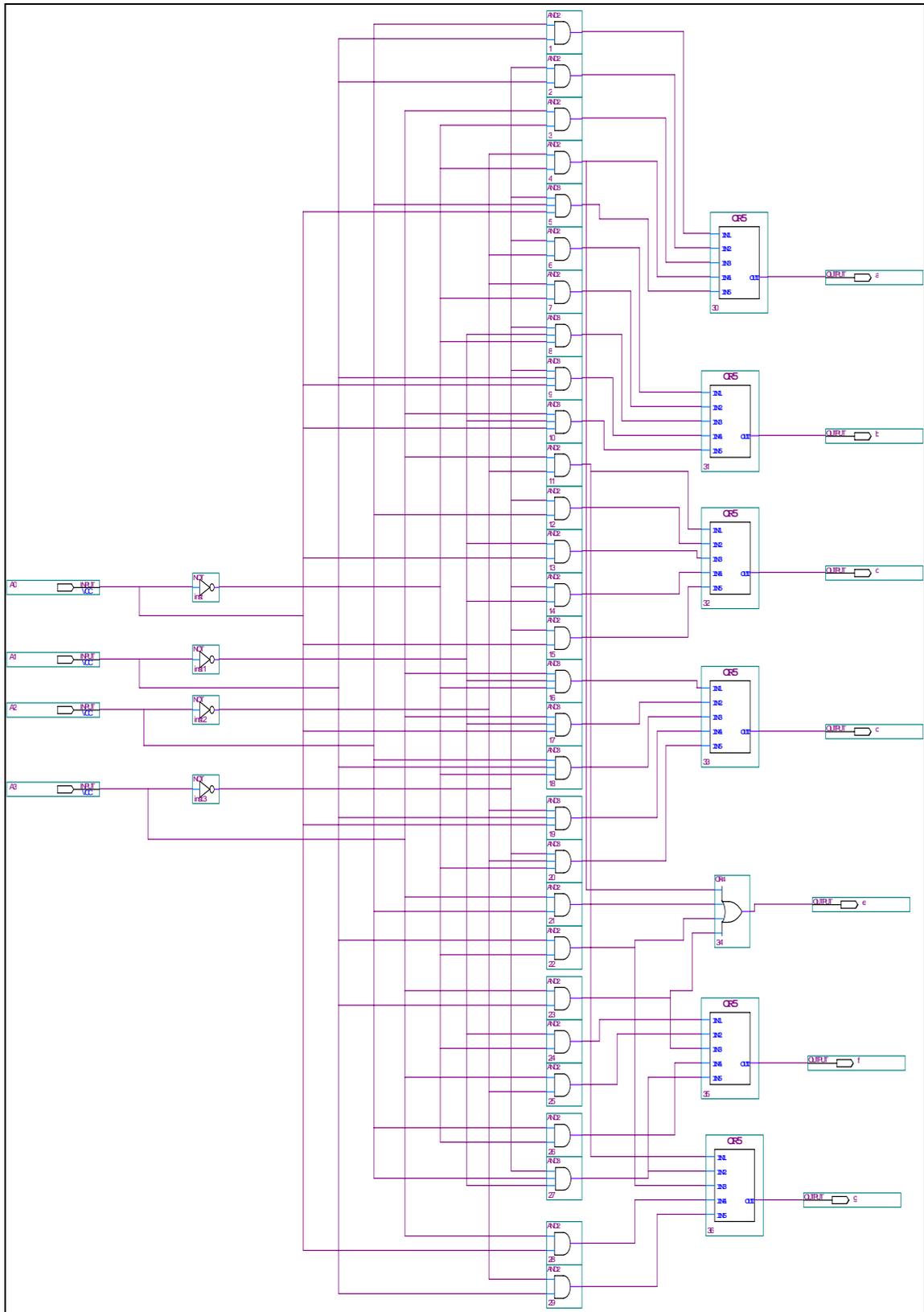


**Appendix A (iii) : 4-bit RCA**



**Appendix A (iv): 17-bits RCA**

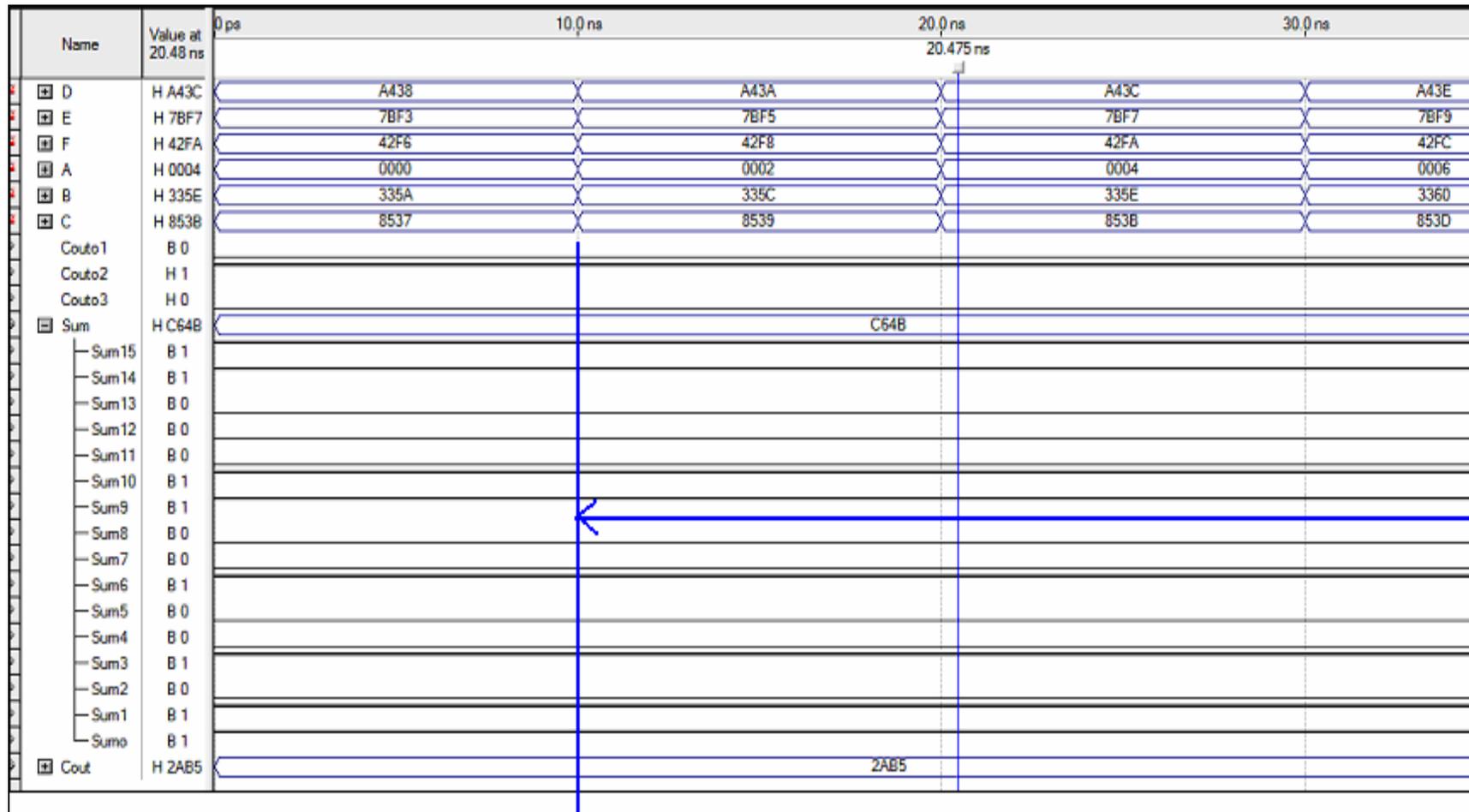
## APPENDIX B



Appendix B(i) : Binary to Seven Segment Decoder

Name	Value at 20.48 ns	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns
				20.475 ns		
D	H A43C	A438	A43A	A43C	A43E	A440
E	H 7BF7	7BF3	7BF5	7BF7	7BF9	7BFB
F	H 42FA	42F6	42F8	42FA	42FC	42FE
A	H 0004	0000	0002	0004	0006	0008
B	H 335E	335A	335C	335E	3360	3362
C	H 853B	8537	8539	853B	853D	853F
Couto1	B 0					
Couto2	H 1					
Couto3	H 0					
Sum	H C673	C64B	C67F	C673	C627	C61B
Cout	H 2AAD	2AB5	2AA1	2AAD	2AD9	2AE5

**Appendix C(i)** : The functional simulation mode of three levels six operands 16-bits CSA design

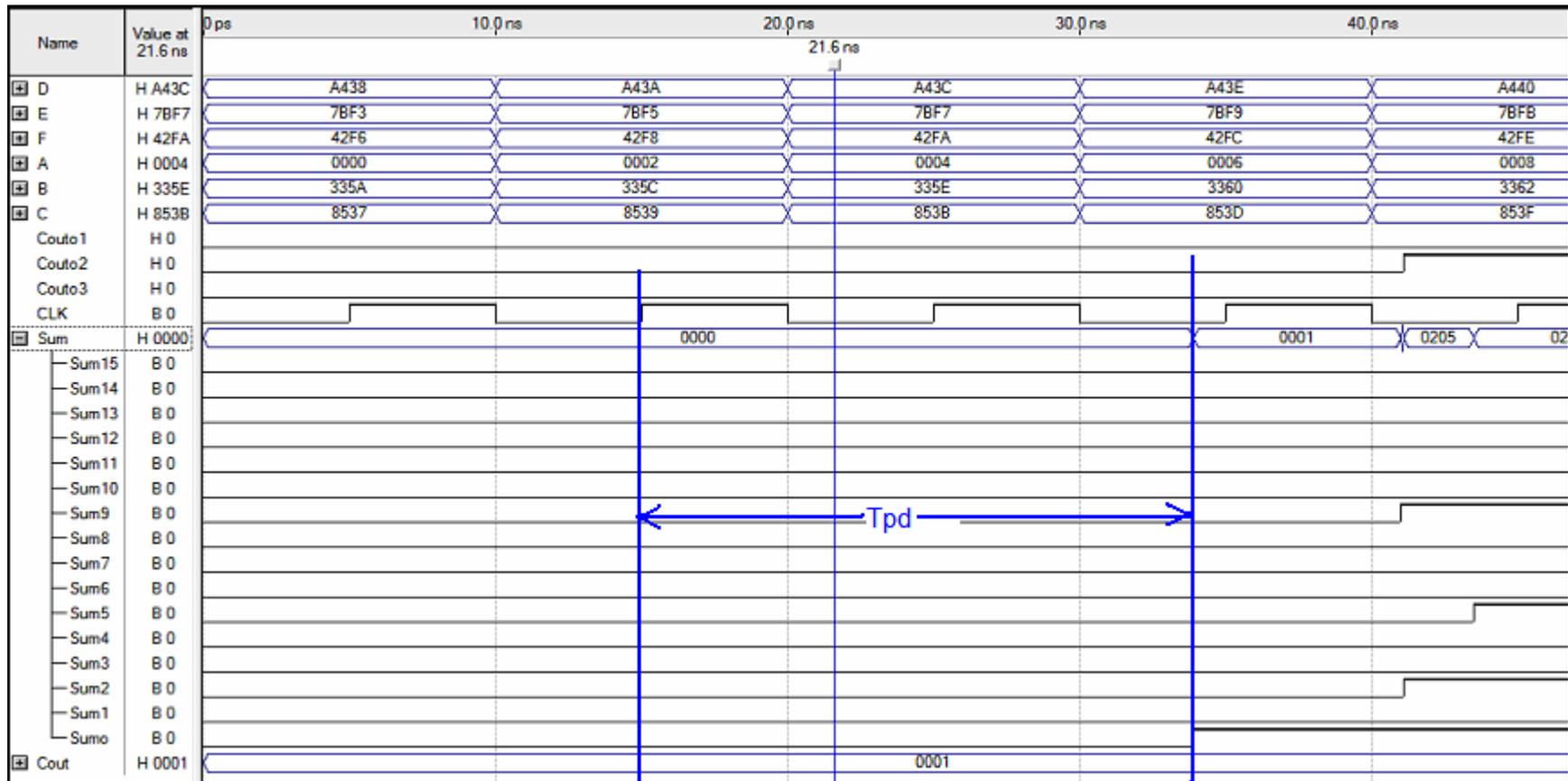


**Appendix C(ii)** : The timing simulation mode of three levels six operands 16-bits CSA design



Name	Value at 21.6 ns	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns
D	H A43C	A438	A43A	A43C	A43E	A440
E	H 7BF7	7BF3	7BF5	7BF7	7BF9	7BFB
F	H 42FA	42F6	42F8	42FA	42FC	42FE
A	H 0004	0000	0002	0004	0006	0008
B	H 335E	335A	335C	335E	3360	3362
C	H 853B	8537	8539	853B	853D	853F
Couto1	H 0					
Couto2	H 0					
Couto3	H 0					
CLK	B 0					
Sum	H 0001	0000	0001	0225	C65F	C673
Cout	H 0001		0001		2AB1	2AAD

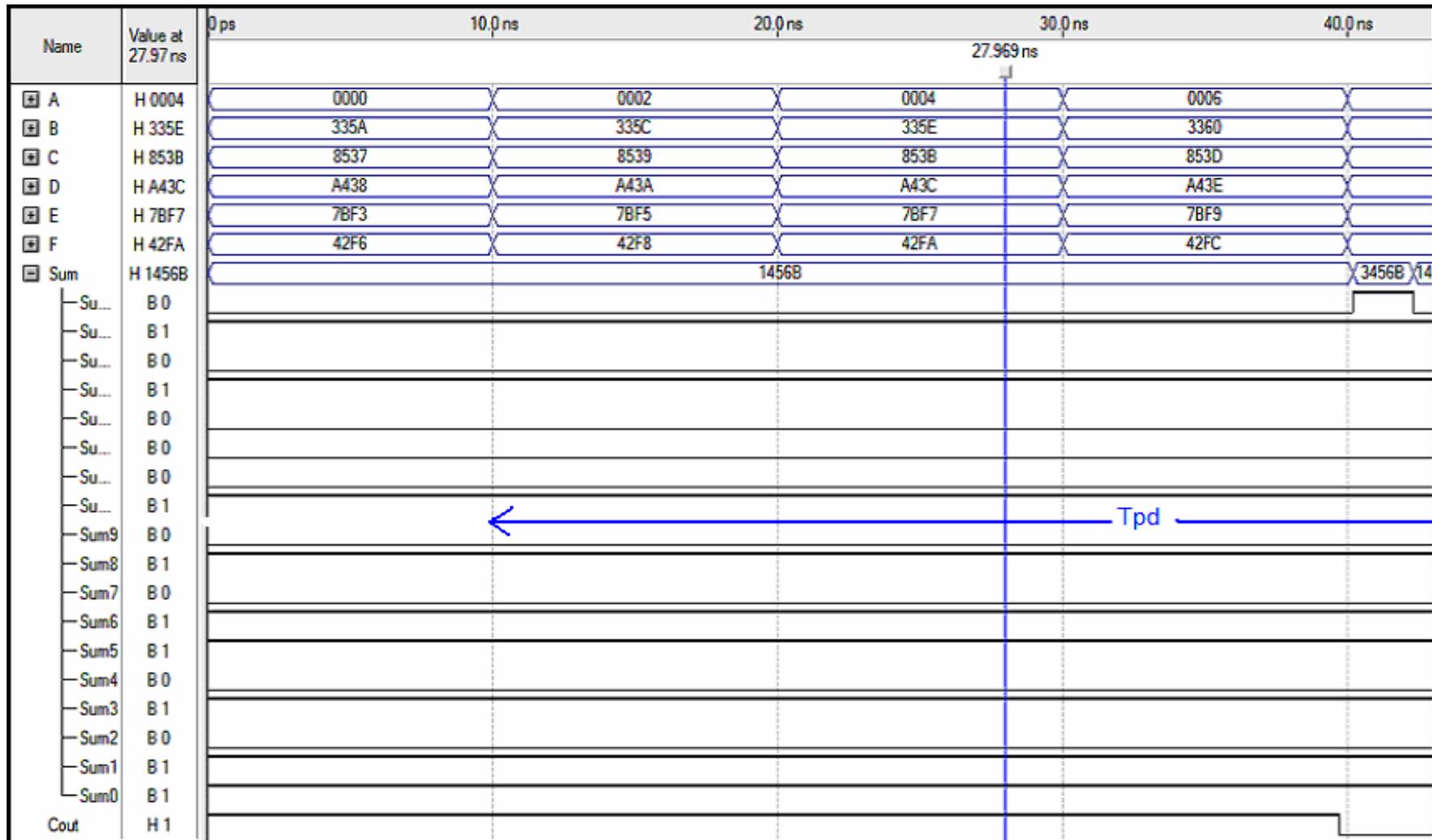
**Appendix C(iv) :** The functional simulation mode of modified of three levels six operands 16-bits CSA design



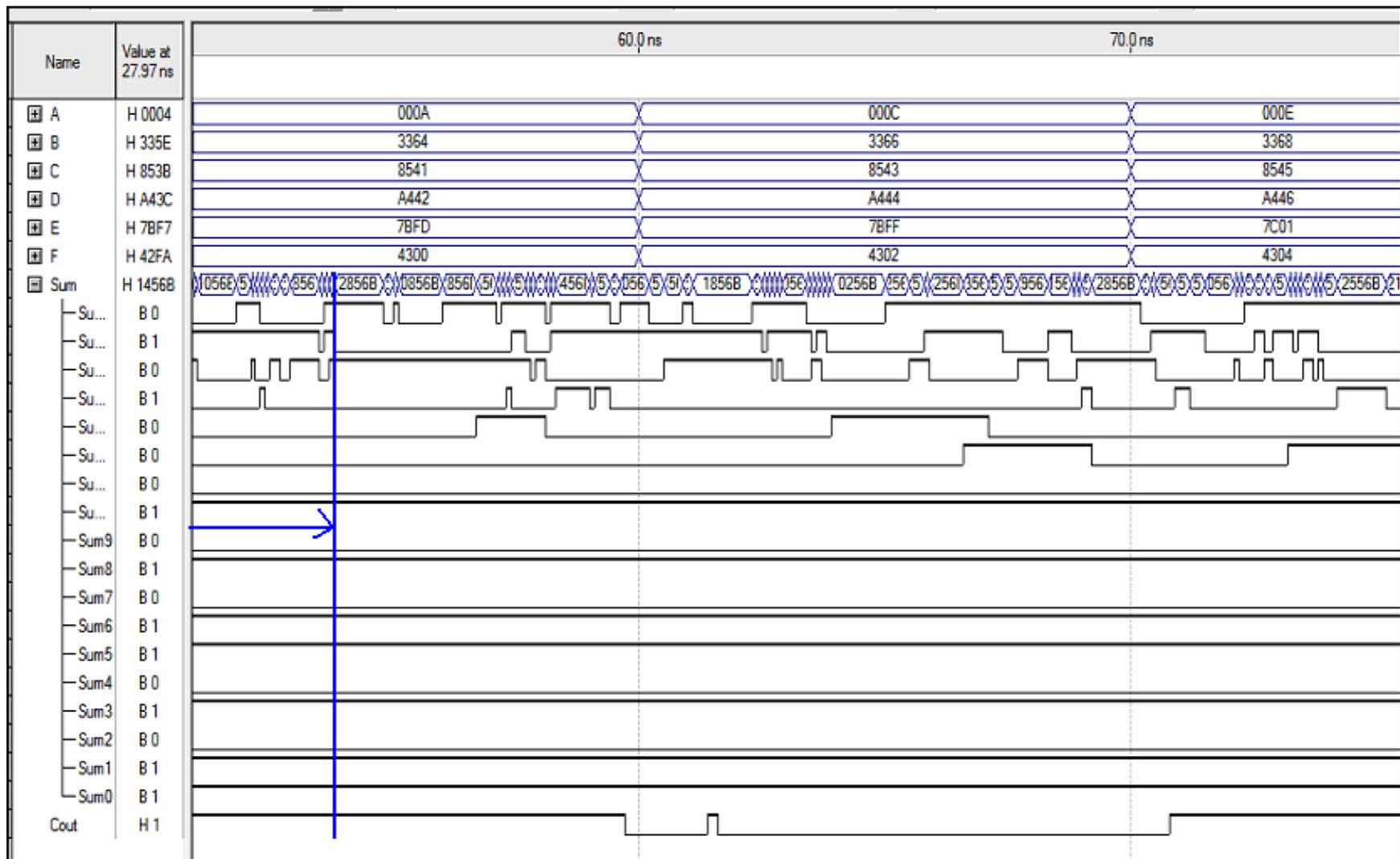
**Appendix C(vi)** : The timing simulation mode of modified three levels six operands 16-bits CSA design

Name	Value at 27.97 ns	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns
					27.969 ns	
A	H 0004	0000	0002	0004	0006	0008
B	H 335E	335A	335C	335E	3360	3362
C	H 853B	8537	8539	853B	853D	853F
D	H A43C	A438	A43A	A43C	A43E	A440
E	H 7BF7	7BF3	7BF5	7BF7	7BF9	7BFB
F	H 42FA	42F6	42F8	42FA	42FC	42FE
Sum	H 2056E	1456B	2856B	2056B	2FD6B	1696B
Cout	H 1					

**Appendix C(vi)** : The functional simulation mode waveform of three levels of six operands 16-bits CSA with RCA



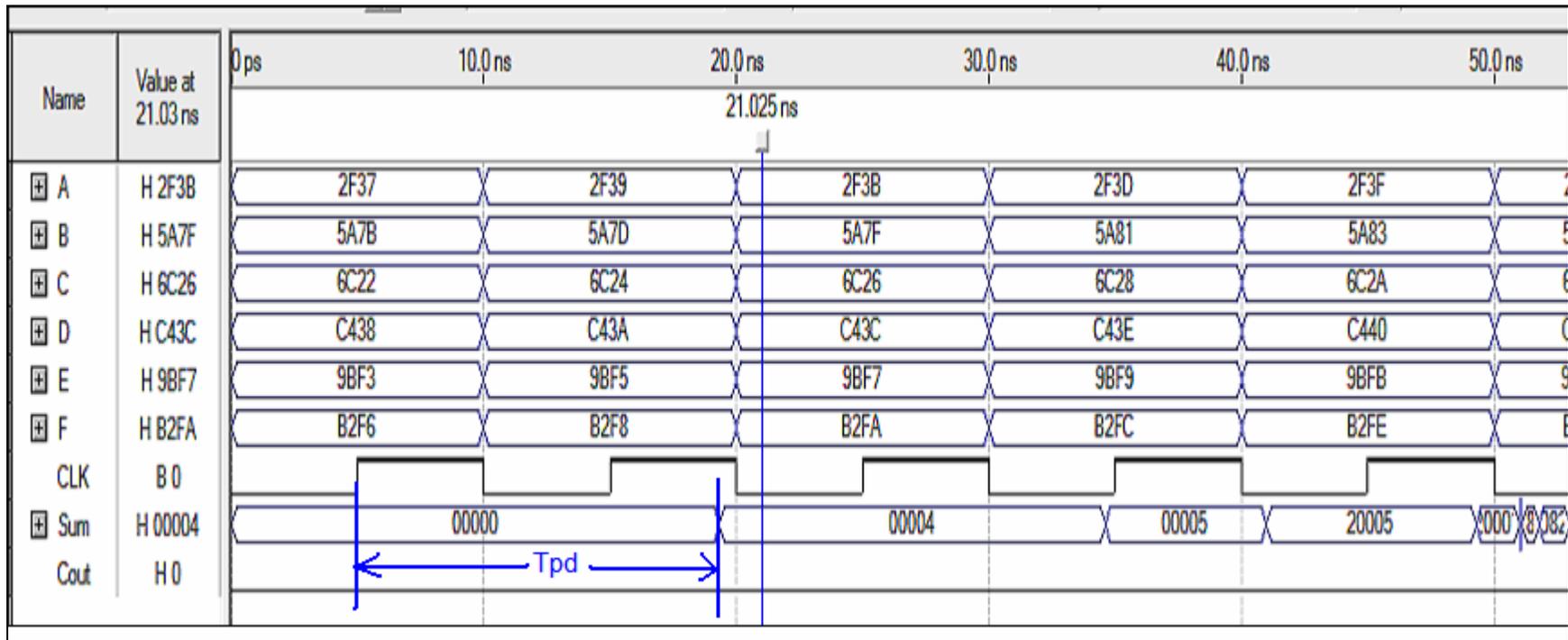
**Appendix C(vii) :** The timing simulation mode waveform of three levels of six operands 16-bits CSA with RCA



**Appendix C(viii)** : The continued timing simulation mode waveform of three levels of six operands 16-bits CSA with RCA

Name	Value at 21.03 ns	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	
CLK	B 0						
A	H 2F3B	2F37	2F39	2F3B	2F3D	2F3F	
B	H 5A7F	5A7B	5A7D	5A7F	5A81	5A83	
C	H 6C26	6C22	6C24	6C26	6C28	6C2A	
D	H C43C	C438	C43A	C43C	C43E	C440	
E	H 9BF7	9BF3	9BF5	9BF7	9BF9	9BFB	
F	H B2FA	B2F6	B2F8	B2FA	B2FC	B2FE	
Sum	H 0000E	00000	00004	00005	20005	2BC6A	
Cout	H 0						

**Appendix C(ix)** : The functional simulation mode of modified three levels six operands 16-bits CSA with RCA design



**Appendix C(x)** : The timing simulation mode of modified of three levels six operands 16-bits CSA with RCA design

## NTE3078 & NTE3079 0.56" Single Digit Numeric Display Seven Segment, RHDP

**Description:**

The NTE3078 (Common Anode) and NTE3079 (Common Cathode) are 0.56 inch (14.2mm) height single digit displays utilizing LED chips which are made from GaAsP on a GaAs substrate.

**Features:**

- 0.56 Inch (14.2mm) Digit Height
- Low Power Requirement
- Excellent Characters Appearance
- Catagorized for Luminous Intensity
- IC Compatible
- Easy Mounting on PC Board or Socket

**Absolute Maximum Ratings:** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

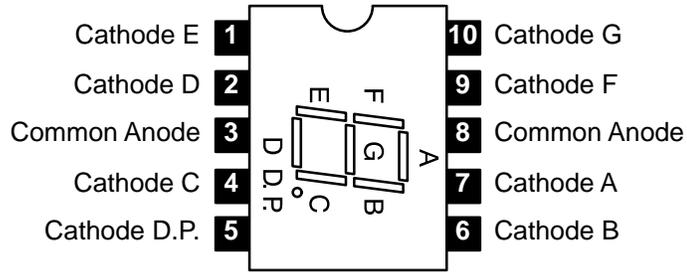
Power Dissipation (Per Segment),  $P_T$  ..... 55mW  
 Peak Forward Current (Per Segment, 1/10 Duty Cycle, 0.1ms Pulse Width),  $I_{Fpeak}$  ..... 160mA  
 Continuous Forward Current (Per Segment),  $I_F$  ..... 25mA  
     Derate Linearly from  $25^\circ\text{C}$  (Per Segment) ..... 0.30mA/ $^\circ\text{C}$   
 Reverse Voltage (Per Segment),  $V_R$  ..... 5V  
 Operating Temperature Range,  $T_{opr}$  .....  $-25^\circ$  to  $+85^\circ\text{C}$   
 Storage Temperature Range,  $T_{stg}$  .....  $-25^\circ$  to  $+85^\circ\text{C}$   
 Lead Temperatue (During Solder, 1/16" Below Seating Plane, 3sec max),  $T_L$  .....  $+260^\circ\text{C}$

**Electrical/Optical Characteristics:** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Average Luminous Intensity	$I_V$	$I_F = 10\text{mA}$	200	500	–	$\mu\text{cd}$
Peak Emission Wavelength	$\lambda_P$	$I_F = 20\text{mA}$	–	655	–	nm
Spectral Line Half-Width	$\Delta\lambda$	$I_F = 20\text{mA}$	–	24	–	nm
Forward Voltage, Any Segment or D.P.	$V_F$	$I_F = 20\text{mA}$	–	1.7	2.0	V
Reverse Current, Any Segment or D.P.	$I_R$	$V_R = 5\text{V}$	–	–	100	$\mu\text{A}$
Luminous Intensity Matching Ratio	$I_{V-m}$	$I_F = 20\text{mA}$	–	–	2:1	

### Pin Connection Diagram

#### NTE3078



#### NTE3079

