CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter discussed about how the data was analyzed until the high-speed design was obtained. From the lowest level designs to the highest-level designs that have been made, the waveforms were analyzed whether it is correct or not based on the CSA truth table (Table 3.1). The results are based on the Quartus II software.

4.2 Result and discussion

4.2.1 Output waveform delay

The result comparison of delay between five full adders designs are shown in Table 4.1. Based on these circuit designs referred to Figure 2.4 until Figure 2.8, the total gates logic of the design influenced the result. The gates logic is differ, but the total number of gates logic being used is same each other. The delay differences can be seen only in the highest-level circuit design. The highest-level circuit design contained four 16-bits CSA in three levels with six operands. Table 4.1 shows the FA waveform based on circuit design.

Table 4.1: Comparison delay between FA circuits design

DESIGN	FA1(ns)	FA2(ns)	FA3(ns)	FA4(ns)	FA5(ns)
FA	10.6	10.6	10.6	10.6	10.6
4-bits CSA	18	18	18	18	18
16-bits CSA	18	18	18	18	18
4-bits RCA	20.4	20.4	20.4	20.4	20.4
17-bits RCA	20.7	20.7	20.7	20.7	20.7
Six operands 16-bits CSA	23.1	23.4	23.4	23.4	23.4
Three levels six operands of 16-bits CSA + RCA	27.9	28.8	28.8	29.1	28.5

This project began by focusing on the full adder (FA) design. Firstly, the waveform output of functional mode simulation has been taken (refer to Figure 4.2) to compare and referred to the truth table in Table 2.1. The outputs design is accurate if the output value met the truth table as shown in Table 2.1. The functional mode simulation waveform output responded at the same time of any changes of inputs. A, B and Ci were the input while the output were Sum and Co. Ci stands for Carry input while Co stands for Carry out. At the second cycle timing, the A input value has changed from 0 to 1 inputs. Hence, the Sum output responded at the same cycle timing and gives the value of 1. Meanwhile the Co responded at 0 value. The marked tpd or also known as delay can be seen at the Sum output at the timing simulation waveform shown in the Figure 4.2. Figure 4.2 shows that the delay is almost 1 cycle. Figure 4.3 shows the longest delay data of FA design.

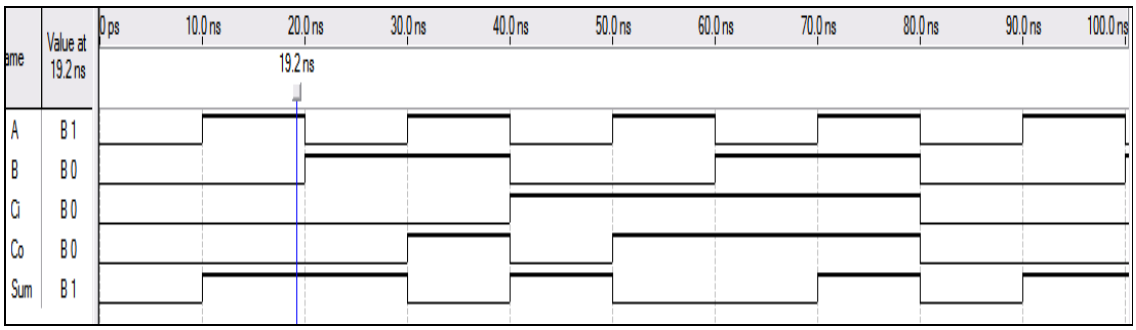

Figure 4.1: The functional simulation mode waveform of FA

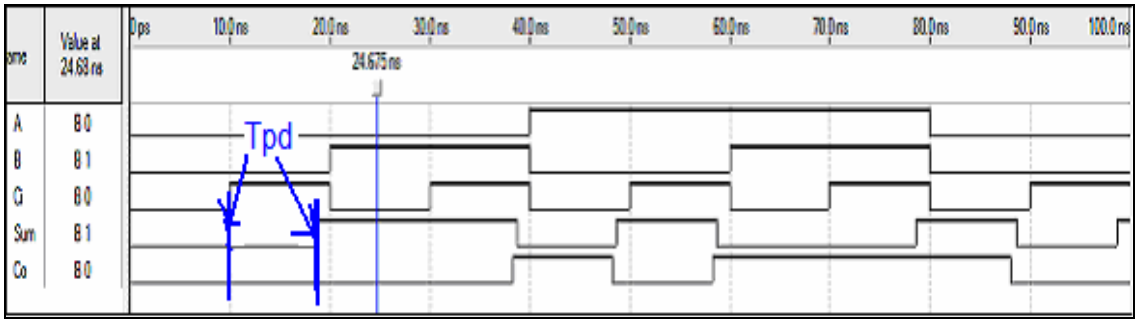

Figure 4.2: The timing simulation mode waveform of FA

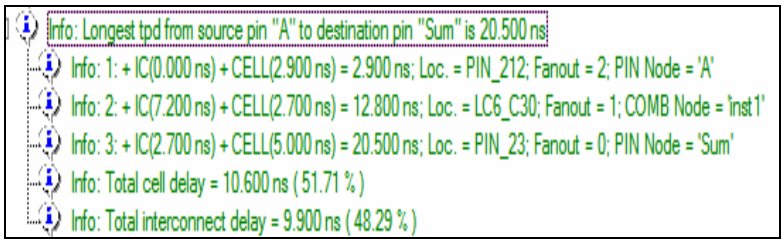

Figure 4.3: Longest delay of FA circuit design

The simulation process of 16-bits CSA produced the functional and timing waveform. The waveform has been compared and checked based on the truth table of 16-bits CSA shown in the Table 3.1 to ensure precisely output. To make it easier for the output to be read and measured, the waveform was first built in functional simulation mode as shown in the Figure 4.4. A, B, and C are the inputs while R and S are the outputs. R stands for Carry Out while S stands for Sum. As mentioned, the outputs change as the changes of inputs. These output values calculated using equation 1.0 and compared to the waveform value. The output waveform value is compatible with the calculated value.

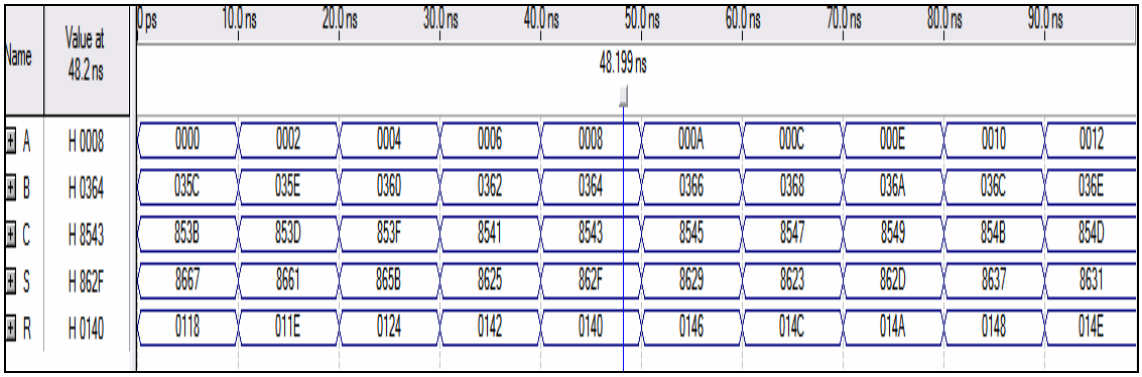

Figure 4.4: The functional simulation mode waveform of 16-bit CSA

Based on Figure 4.5, the delay output can be seen clearly at the marked Tpd. At the first cycle of inputs, the output values are remains as same as the output value at the previous cycle. Thus, the change of output value at the first cycle input cannot be seen. At the second cycle of inputs the outputs responded at the fourth cycle period. This delay has been referred and compared to the Figure 4.4 to ensure to get the accurate value. Compared between Figure 4.5 and Figure 4.4, there are different delays of each output but the outputs at Sum and Carry out is similarly. The output waveform value in the Figure 4.5 cannot be considered until it meet the same value as in the Figure 4.4. This is the reason why the functional waveform has to read first to avoid misread value being taken in the timing simulation mode.

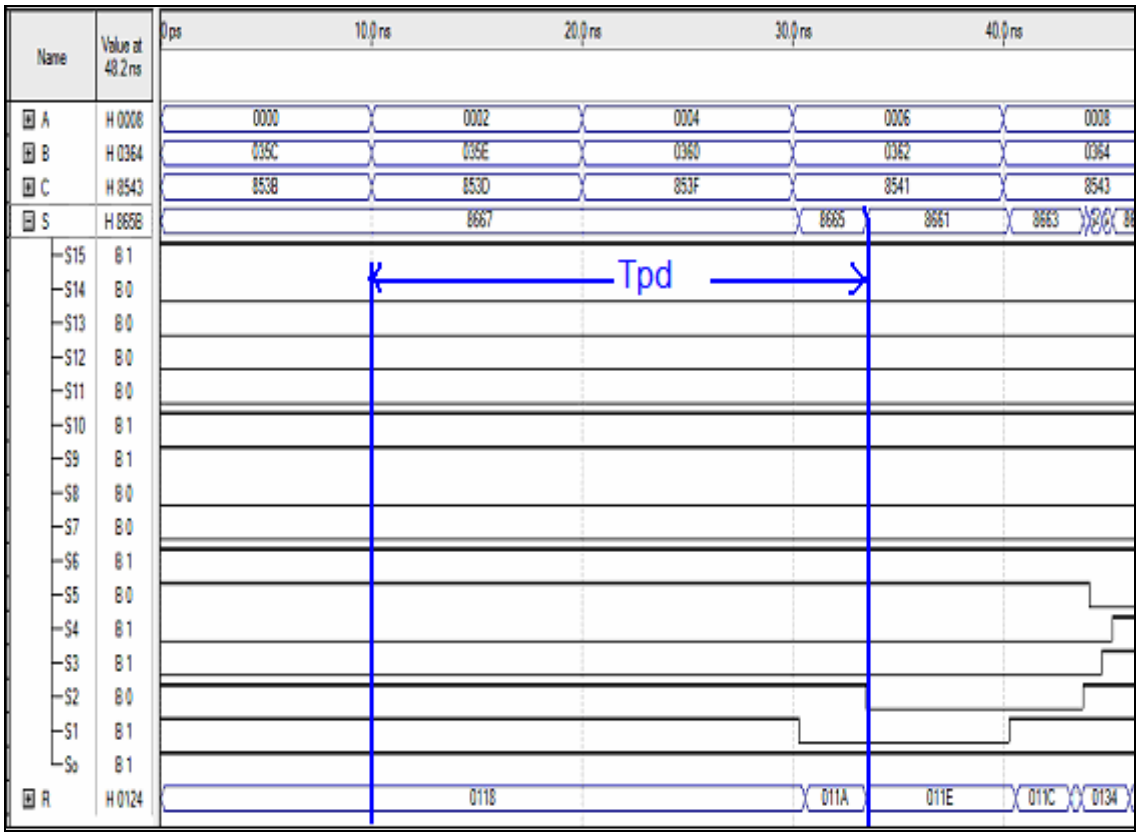

Figure 4.5: The timing simulation mode waveform of 16-bits CSA

The longest delay of 16-bits CSA data can be seen in the Figure 4.6.

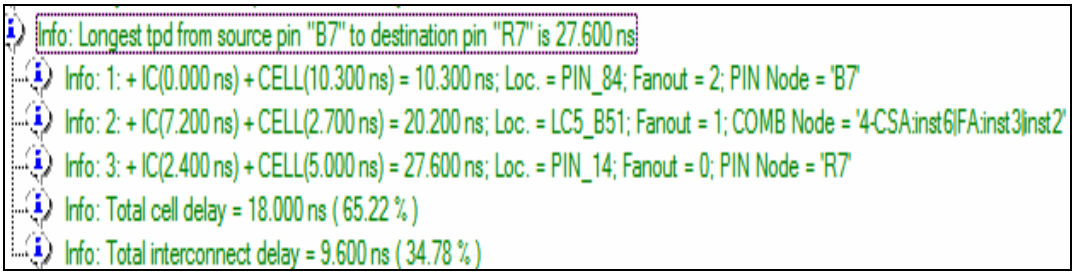

Figure 4.6: The longest delay of 16-bits CSA

The simulation process of six operands of 16-bits CSA produced the functional and timing waveform. The waveforms can be seen in Appendix D (i), Appendix D (ii) and Appendix D (iii). The waveform has been compared and checked based on the truth table of 16-bits CSA shown in the Table 3.1 to ensure precisely output.

The simulation process of three levels six operands of 16-bits CSA with RCA produced the functional and timing waveform. The waveforms can be seen in Appendix D (vii) and Appendix D (vii).

The difference of basic design and modified design waveform is the existence of clock. The simulation process of modified 16-bits CSA produced the functional and timing waveform.

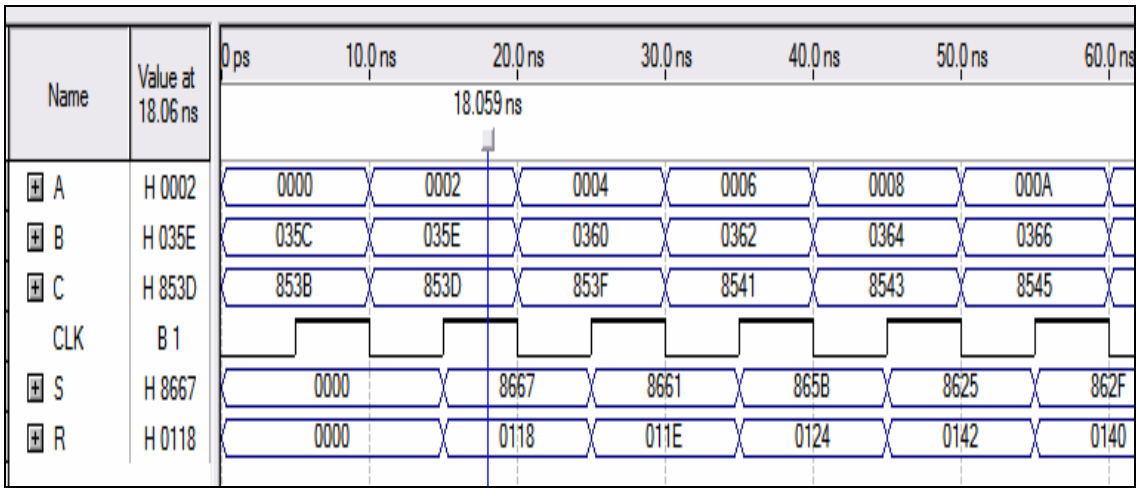

Figure 4.7: The functional simulation mode waveform of modified 16-bits CSA

Figure 4.7 shows the output responded at the positive-edge clock based of the used of D flip-flop. At the Figure 4.7, the first timing cycle outputs responded at the positive edge clock at its cycle and so on.

Differ with figure 4.8, the outputs of first cycle period inputs are responded after the third positive edge clock. The delay is about one and half cycle clock. The delay or Tpd can be seen in the Figure 4.8. Each output's delay is different but the precisely output can be identified by the comparison of Figure 4.7 output waveform. The longest delay of this circuit can be seen in the Figure 4.9.

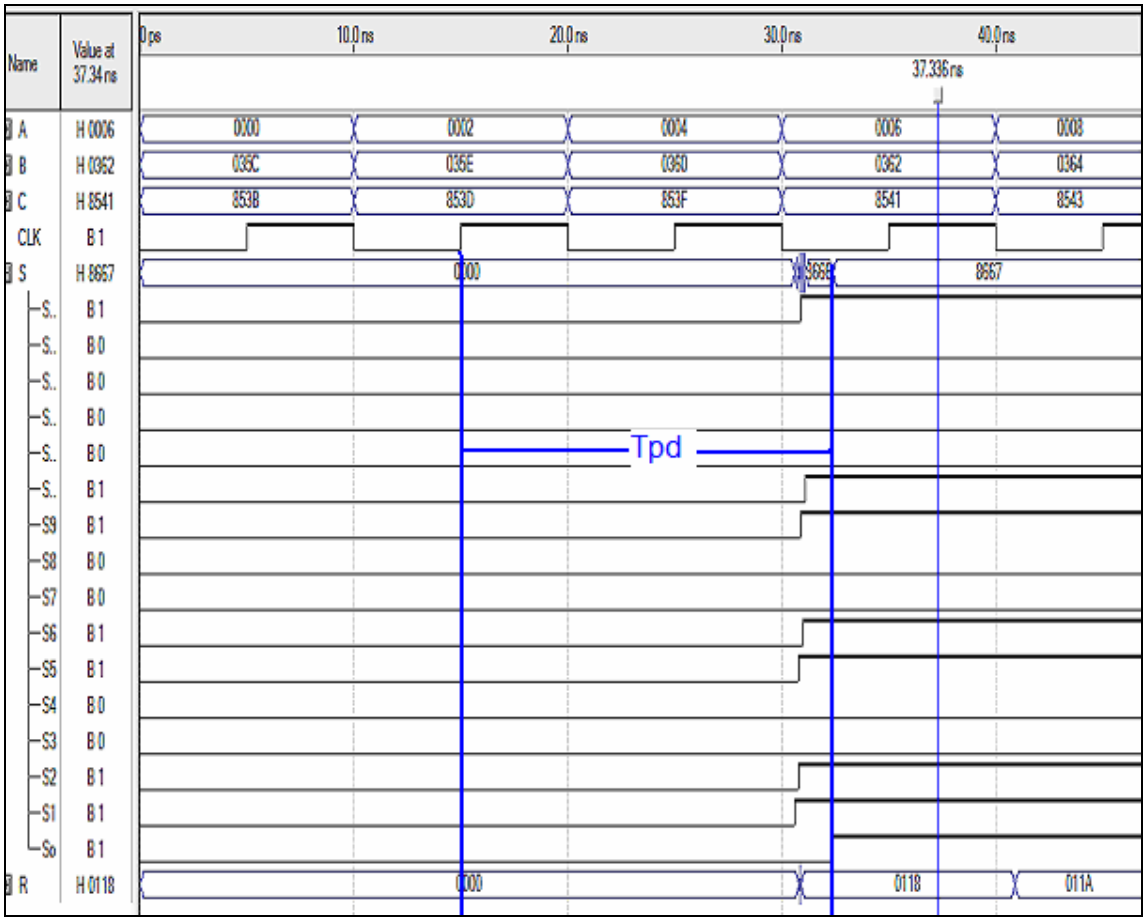

Figure 4.8: The timing simulation mode waveform of modified 16-bit CSA

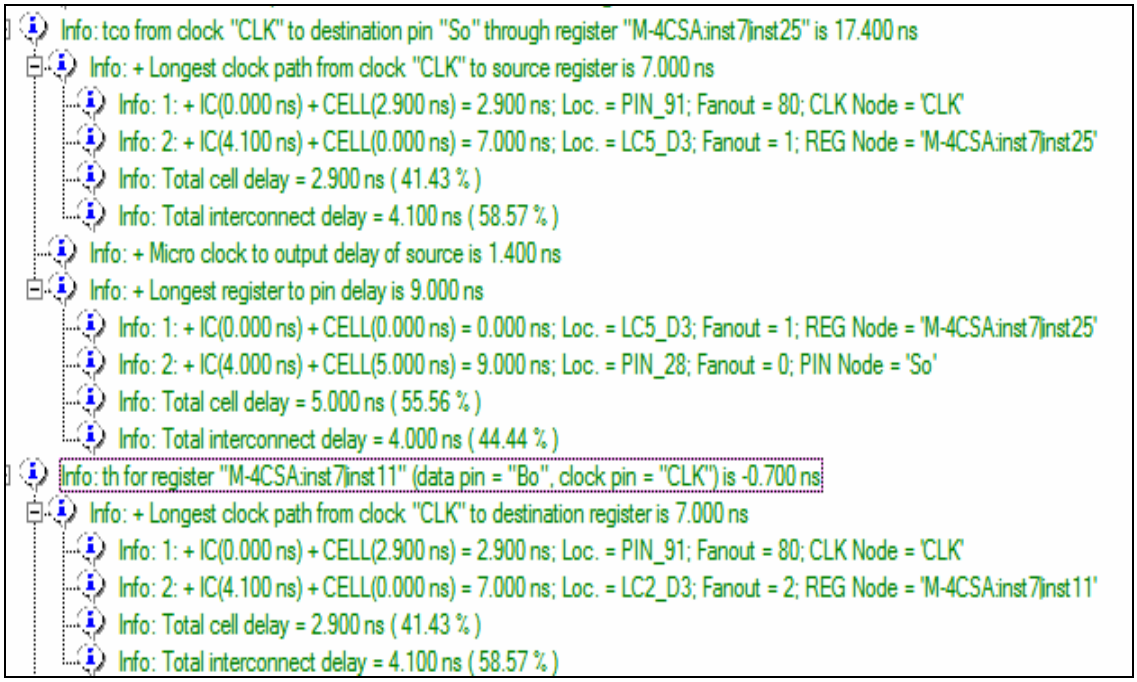

Figure 4.9: The longest delay of modified 16-bits CSA

The simulation process of modified six operands of 16-bits CSA produced the functional and timing waveform. The waveforms can be seen in Appendix D (iv) and Appendix D (v). Meanwhile the simulation process of modified three levels six operands of 16-bits CSA with RCA produced the functional and timing waveform. The waveforms can be seen in Appendix D (ix) and Appendix D (x).

4.2.2 Speed

Based on the Figure 4.10, the basic design speed has been measured. The difference of both the major design of this project, in basic design circuit, referred to the Figure 4.10 and modified design circuit, referred to the Figure 4.12 is 73.25MHz. The existence of pipeline proved that the design could be speed up.

	Value
From	1IN-16BITX5-DLATCH:inst|1IN-16BIT-DLATCH:inst3|1IN-4B...
To	1IN-3BIT-DLATCH:inst5|inst9
Clock period	59.400 ns
Frequency	16.84 MHz

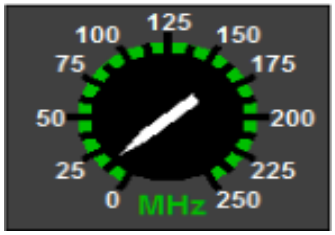

Figure 4.10: Speed of non-pipelined three level 16-bit CSA with RCA

Based on the Figure 4.11 and figure 4.12, the addends of gates logic of RCA in the Figure 4.12 decrease 0.9%. This modified high-speed design used four stages of pipelining.

Refer to the Figure 3.8 and Figure 3.9, the pipeline do not put at the RCA stage. This is because of the pipeline does not have to exist at each stages of design, but depends on its needed. The unused of existence D flip-flop would decrease its speed while increased the number of hardware used and increased its cost.

	Value
From	M-16CSA:inst3|M-4CSA:inst5|inst19
To	2IN-16BIT-DLATCH:inst1|2IN-4BIT-DLATCH:inst2|inst3
Clock period	11.000 ns
Frequency	90.91 MHz

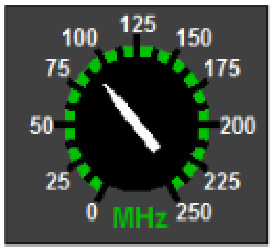

Figure 4.11: Speed of modified Six operands of 16-bits CSA

	Value
From	M-6OPERAND16-BITCSA:inst2|2IN-16BIT-DLATCH:inst1|2I...
To	M-6OPERAND16-BITCSA:inst2|2IN-16BIT-DLATCH:inst5|2I...
Clock period	11.100 ns
Frequency	90.09 MHz

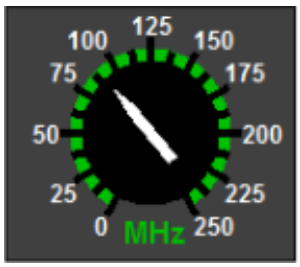

Figure 4.12: Speed of modified three level of 6 operands 16-bit CSA with RCA

4.3 Conclusion

Based on the analysis in this chapter, the data can be concluding as shown in the Table 4.2. Since the design is in the basic, the delay can be measured. The complex the design, the bigger delay. Since the existence of clock in the circuit design, the speed can be measured. The speed increases rapidly with the existence of pipeline at each stages of circuit design.

Table 4.2: The analysis data throughout achieves design

DESIGN	Delay(ns)	Speed (MHz)
FA	10.6	-
4-bits CSA	18	-
16-bits CSA	18	-
4-bits RCA	20.4	-
17-bits RCA	20.7	-
Six operands 16-bits CSA	23.1	-
Three levels six operands 16-bits + RCA	27.9	-
Non-pipelined three levels six operands 16-bits + RCA	-	16.84
Modified Six operands 16-bits CSA	-	90.91
Modified three levels Six operands 16-bits + RCA	-	90.09