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Development of varied CMOS ring oscillator topologies in 0.13-Î¼m CMOS technology

Abstract

This paper presents varied CMOS ring oscillator topologies using Silterra 0.13-µm Process. Three topologies of ring oscillators have been designed which is the single-ended ring oscillator, differential ring oscillator and ring oscillator based variable resistor for 2.4 GHz wireless applications. The proposed designs consist of five stages delay cell. The simulation results show that a single-ended ring oscillator obtained the lowest power consumption of 0.41 mW, while differential oscillator achieves phase noise of −64.44 dBc/Hz at 1 MHz offset frequency. However, ring oscillator based variable resistor did not achieve any significant improvement. The proposed design is oscillates at 2.4 GHz.

Keywords; Delay Cell, Phase Noise, Ring Oscillator, Variable Resistor