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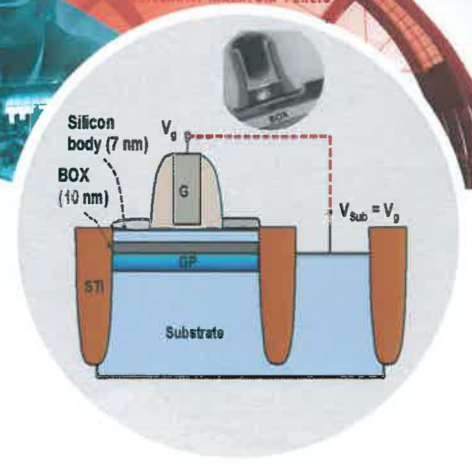


INVENTORS

DR. MOHD KHAIRUDDIN MD ARSHAD
PROF. DR. UDA HASHIM
NORAINI OTHMAN

CONTACT DETAILS

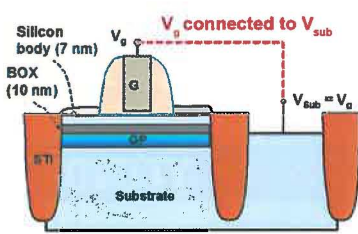
INSTITUTE OF NANO ELECTRONIC ENGINEERING (INEE)
UNIVERSITI MALAYSIA PERLIS
01000 KANGAR, PERLIS
Telephone : 049797836
email : mohd.khairuddin@unimap.edu.my

ASYMMETRICAL DOUBLE GATE:

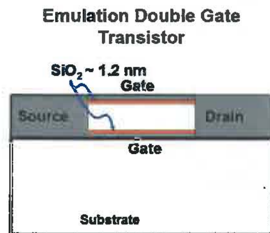
SIGNIFICANT IMPROVEMENT IN ULTRA-SCALED SOI MOSFET

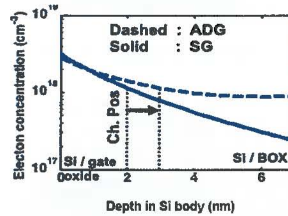
INTRODUCTION

Fully-depletion operation is mandatory requirement for ultra-scaled devices (i.e. < 45 nm technology) which only can be achieved either multi-gate (i.e. FinFET) or thin body Silicon-on-Insulator (SOI). Thin body SOI offers another interesting feature compared to any other technologies i.e. back-gate biasing. In this invention, we utilize asymmetrical contact from the top which provide improved performance and better controlled of short-channel effects in thin body and thin buried oxide of SOI MOSFETs.



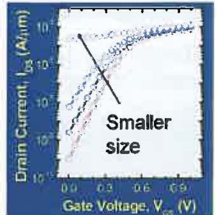
Emulation Double Gate Transistor





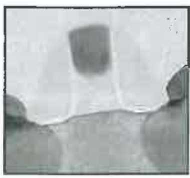
Elimination Short Channel Effects

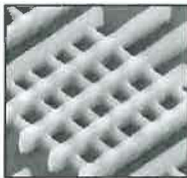
Short Channel Effects

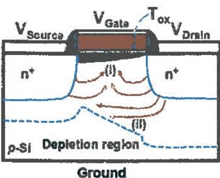


NOVELTY

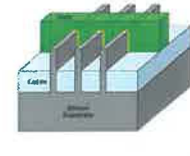
Existing Technologies | **New Invention**



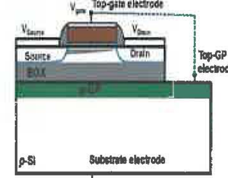




Planar Architecture – Silicon Platform



3D Architecture – Silicon/ SOI Platform



Planar Architecture – SOI Platform

- Simple architecture with significant Improvement on drive current (Id-Vg and Id-Vd) without forgo the off current.
- Extension to ultra-scaled devices : support Moore's Law for ~ 10 nm technology
- Eliminate Short Channel Effects

Collaboration

- Université catholique de Louvain, Louvain-la-neuve, Belgium
- CEA – Leti, Grenoble, France

PUBLICATIONS

- M.K. Md Arshad et al, Solid-State Electronics, 2014 (accepted for publication)
- M.K. Md Arshad et al, Solid-State Electronics, 90, 2013: 56-64
- M.K. Md Arshad et al, IEEE Trans. Electron Devices, 59, 2012: 247-251
- M.K. Md Arshad et al, Solid-State Electronics, 90, 2012: 50-58
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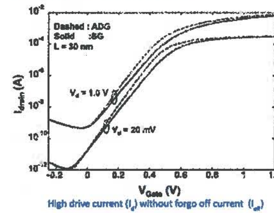
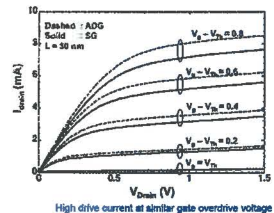
- M.K. Md Arshad et al, Solid-State Electronics, 54, 2010: 213 - 219

RESULTS

I-V Characteristics



High drive current (I_d) without forgo off current (I_{off})



High drive current at similar gate overdrive voltage

COMMERCIALIZATION POTENTIAL

* 22 nm gate length	Single Gate	Asymmetrical Double Gate	% improvement
V_{Th} (V)	0.45	0.30	30 %
SS (mV/dec)	95	80	15 %
DIBL (mV/V)	115	95	18 %
Ion (uA/um)	500	620	24 %

- Lower threshold voltage (i.e suitable for low power application –energy saving)
- Lower subthreshold slope (i.e faster switching speed between on and off),
- Lower drain-induced barrier lowering (i.e. better control of short channel effects : translated into ~ 20 % increased in speed.

PRODUCT IMPLEMENTATION

Low power mobile application i.e. smart phone.

Knowledge • Sincerity • Excellence