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HIGH PERFORMANCE VIDEO GRAPHIC ARCHITECTURE USING HYBRID LOGARITHMIC SYSTEM

PATENT SEARCH NO.: PT4502

INTRODUCTION

It is known that the engines generate an image from a scene described as a list of vertices, a list of triangles and the position of the camera. The transformation stage transforms the vertices from the scene coordinates to the camera's viewing frustum coordinates, including perspective computations. Typically, this stage is very sensitive, as it determines the on-screen position of the triangles, and therefore requires some precision so as not to distort the objects, and will also involve repetitive arithmetic operations.

NOVELTY

The hybrid logarithmic number system (LNS) is proposed as an alternative to conventional floating-point (FLP) system for computing arithmetic functions.

TECHNICAL VALUES

In comparison to using conventional FLP system:

- High speed
- Reduce area
- Better accuracy

PUBLICATIONS

- R.C Ismail, M.K Zakaria, S.A.Z Murad, "Hybrid Logarithmic Number System Arithmetic Unit: A Review", IEEE International Conference on Circuits and Systems, pp. 55-58, 2013.
- R.C Ismail, J.N Coleman, S.A.Z Murad, R. Hussin, "Improved Subtraction Function for Logarithmic Number System", Malaysian Technical Universities Conference on Engineering and Technology, pp. 151-155, 2012. (Best Paper for Industry Award Category)
- R.C Ismail, R. Hussin, S.A.Z Murad,"Interpolator Algorithms for Approximating LNS Addition and Subtraction: Design Analysis", IEEE International Conference on Circuits and Systems, pp. 174-179 2012.

Fig. 1: FLP 14 bits

Fig. 2: Hybrid LNS 14 bits

Fig. 3: FLP 16 bits

Fig. 4: Hybrid LNS 16 bits

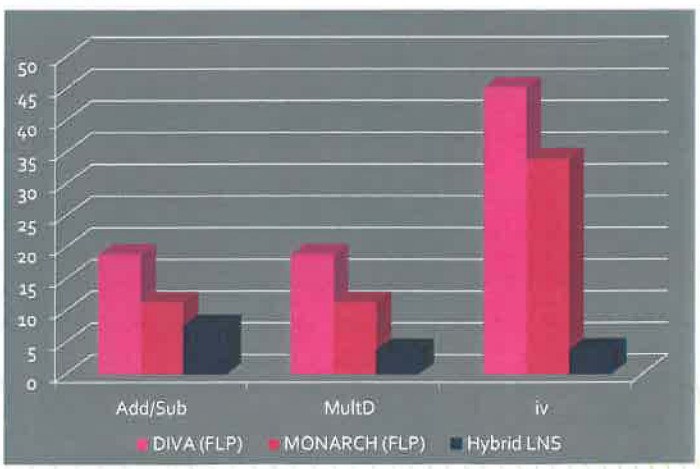

Fig. 5: Delay times in nanoseconds (ns).

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- R.C Ismail, J.N Coleman, "ROM-less LNS", 20th IEEE Symposium on Computer Arithmetic (ARITH), pp. 43-51, 2011.
- J. N. Coleman, C. I. Softley, J. Kadlec, R. Matousek, M. Tichy, Z. Pohl, A. Hermanek, N. F. Benschop, "The European Logarithmic Microprocessor", IEEE Transactions on Computers, pp. 532-546, 2008.