COMPARISON OF DELAYS BETWEEN 4-BITS RIPPLE-CARRY ADDER AND 4-BITS CARRY LOOK-AHEAD ADDER USING LOGICAL EFFORT METHOD

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APPROVAL AND DECLARATION SHEET

This project report titled Comparison of Delays Between 4-Bits Ripple-Carry Adder And 4-Bits Carry Look-Ahead Adder Using Logical Effort Method was prepared and submitted by Siti Nurhanani Binti Che Yahaya (Matrix number: 071010934) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Microelectronic Engineering) in University Malaysia Perlis (UniMAP).

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MEMBANDINGKAN LENGAH DI ANTARA LITAR PENAMBAH PEMBAWA RIAK 4-BIT DAN LITAR PENAMBAH PEMBAWA LIHAT-KE-HADAPAN DENGAN MENGGUNAKAN KAEDAH KEUPAYAAN LOGIK

ABSTRAK

Dalam projek ini telah direka dua jenis litar yang berbeza iaitu litar Penambah Pembawa Riak 4-bit (PBR) dan litar Penambah Pembawa Lihat-Ke-Hadapan 4-bit (PBLH). Lengah dalam litar PBR 4-bit dibandingkan diantara sebelum dan selepas mengaplikasikan kaedah Keupayaan Logik, untuk menentukan litar yang paling bagus dari segi mempunyai tindak-balas yang cepat antara masukan dan keluaran. Selain itu litar PBR akan dibandingkan dengan PBLH untuk menunjukkan bahawa dua litar yang berbeza dengan fungsi yang sama mempunyai lengah yang berbeza. Dalam kaedah Keupayaan Logik, terdapat beberapa langkah yang digunakan seperti pengiraan keupayaan laluan, pengiraan bilangan peringkat logic, anggaran lengah yang minima, menentukan keupayaan peringkat yang terbaik, dan penentuan saiz get dalam litar PBR. Dalam projek ini dapat dilihat bagaimana hasil dari mengaplikasi kaedah Keupayaan Logik memberikan lengah yang singkat berbanding sebelum kaedah itu diaplikasikan iaitu sekitar 44.15% pembaikan. Manakala peratusan purata pembaikan PBLH berbanding PBR adalah sekitar 64.85%, yang menunjukkan topologi litar yang berbeza akan mempunyai lengah yang berbeza. Semakin kompleks sesuatu litar (mempunyai bilangan masukan yang banyak) semakin tinggi lengahnya. Bilangan get tidak mempengaruhi lengah dalam litar yang mana kadang-kadang dengan mempunyai bilangan get yang lebih banyak boleh memulihkan lagi lengah litar.

COMPARISON OF DELAYS BETWEEN 4-BITS RIPPLE-CARRY ADDER CIRCUIT AND 4-BITS CARRY LOOK-AHEAD ADDER CIRCUIT BY USING LOGICAL EFFORT METHOD

ABSTRACT

In this project, two types of circuit topologies has been designed which are the 4-Bits Ripple-Carry Adder Circuit (RCA) and the 4-Bits Carry Look-Ahead Adder Circuit (CLA). Delays in RCA circuit will be compared between before and after applying the Logical Effort method to determine which circuit is good in terms of having a faster response between input and output. Besides, RCA circuit also will be compared with CLA circuit to show that different circuit topologies with the same circuit function would have different circuit delays. The Logical Effort method, includes some steps such as path effort computation, best number of stages computation, minimum delay estimation, best stage effort determination and sizing the gates in the RCA circuit. In this project, after applying the Logical Effort method, the circuit will have less delays compared to the same circuit that does not apply Logical Effort, with an improvement is about 44.15%. Meanwhile, the average improvement of CLA over RCA is about 64.85%, which means different circuit topologies would have different delays. The more complex a circuit is (high fan-in) it produces more delays. Gates number did not affected the delays in a circuit which sometimes, by having addition stages with same circuit function would improved the delays and produced fast response circuit.

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