

COMPARISON OF DELAYS BETWEEN 4-BITS RIPPLE-CARRY ADDER AND 4-BITS CARRY LOOK-AHEAD ADDER USING LOGICAL EFFORT METHOD

SITI NURHANANI BINTI CHE YAHAYA

Report submitted in partial fulfillment
of the requirements for the degree
of Bachelor of Engineering



JUNE 2011

COMPARISON OF DELAYS BETWEEN 4-BITS
RIPPLE-CARRY ADDER AND 4-BITS CARRY LOOK-
AHEAD ADDER USING LOGICAL EFFORT METHOD

SITI NURHANANI BINTI CHE YAHAYA

SCHOOL OF MICROELECTRONIC ENGINEERING
UNIVERSITI MALAYSIA PERLIS

2011

© This item is protected by original copyright

ACKNOWLEDGEMENT

A special thanks goes to my helpful supervisor Mrs Norina Binti Idris, who is pleasantly encouraging, giving guidance and advise mentally during all this period to finish my project. The supervision and support that she gave truly helps the progress and confirmity of the project. The co-operation is much indeed appreciated. This project would be nothing without the enthusiasm and imagination from her.

I also would like to thank my friends, Wong Liang Yuan, Kau Zhee Shuan, Chiew Chee Ting and Mohd Amin Jamain for being nice, patient and has contributed great help to me regarding the Mentor Graphics software and sharing ideas about my project title 'Comparison Of Delays Between 4-Bits Ripple-Carry Adder Circuit And 4-Bits Carry Look-Ahead Adder Circuit By Using Logical Effort Method'.

My appreciation also goes to my family for the supports and encouragement throughout my academic life. Last but not least, thanks to all my lectures in the School of Microelectronic Engineering for the contribution throughout my 4 years study. Thank you also for librarians, engineers, laboratory, technicians, and all staffs in School of Microelectronic Engineering for those appreciated helps all this while.

APPROVAL AND DECLARATION SHEET

This project report titled Comparison of Delays Between 4-Bits Ripple-Carry Adder And 4-Bits Carry Look-Ahead Adder Using Logical Effort Method was prepared and submitted by Siti Nurhanani Binti Che Yahaya (Matrix number: 071010934) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Microelectronic Engineering) in University Malaysia Perlis (UniMAP).

Checked and Approved by

(Mrs. Norina Binti Idris)

Project Supervisor

**School of Microelectronic Engineering
University Malaysia Perlis**

June 2011

MEMBANDINGKAN LENGAH DI ANTARA LITAR PENAMBAH PEMBAWA RIAK 4-BIT DAN LITAR PENAMBAH PEMBAWA LIHAT-KE-HADAPAN DENGAN MENGGUNAKAN KAEDAH KEUPAYAAN LOGIK

ABSTRAK

Dalam projek ini telah direka dua jenis litar yang berbeza iaitu litar Penambah Pembawa Riak 4-bit (PBR) dan litar Penambah Pembawa Lihat-Ke-Hadapan 4-bit (PBLH). Langkah dalam litar PBR 4-bit dibandingkan diantara sebelum dan selepas mengaplikasikan kaedah Keupayaan Logik, untuk menentukan litar yang paling bagus dari segi mempunyai tindak-balas yang cepat antara masukan dan keluaran. Selain itu litar PBR akan dibandingkan dengan PBLH untuk menunjukkan bahawa dua litar yang berbeza dengan fungsi yang sama mempunyai langkah yang berbeza. Dalam kaedah Keupayaan Logik, terdapat beberapa langkah yang digunakan seperti pengiraan keupayaan laluan, pengiraan bilangan peringkat logic, anggaran langkah yang minima, menentukan keupayaan peringkat yang terbaik, dan penentuan saiz get dalam litar PBR. Dalam projek ini dapat dilihat bagaimana hasil dari mengapikasi kaedah Keupayaan Logik memberikan langkah yang singkat berbanding sebelum kaedah itu diaplikasikan iaitu sekitar 44.15% pembaikan. Manakala puratusan purata pembaikan PBLH berbanding PBR adalah sekitar 64.85%, yang menunjukkan topologi litar yang berbeza akan mempunyai langkah yang berbeza. Semakin kompleks sesuatu litar (mempunyai bilangan masukan yang banyak) semakin tinggi lengahnya. Bilangan get tidak mempengaruhi langkah dalam litar yang mana kadang-kadang dengan mempunyai bilangan get yang lebih banyak boleh memulihkan lagi langkah litar.

COMPARISON OF DELAYS BETWEEN 4-BITS RIPPLE-CARRY ADDER CIRCUIT AND 4-BITS CARRY LOOK-AHEAD ADDER CIRCUIT BY USING LOGICAL EFFORT METHOD

ABSTRACT

In this project, two types of circuit topologies has been designed which are the 4-Bits Ripple-Carry Adder Circuit (RCA) and the 4-Bits Carry Look-Ahead Adder Circuit (CLA). Delays in RCA circuit will be compared between before and after applying the Logical Effort method to determine which circuit is good in terms of having a faster response between input and output. Besides, RCA circuit also will be compared with CLA circuit to show that different circuit topologies with the same circuit function would have different circuit delays. The Logical Effort method, includes some steps such as path effort computation, best number of stages computation, minimum delay estimation, best stage effort determination and sizing the gates in the RCA circuit. In this project, after applying the Logical Effort method, the circuit will have less delays compared to the same circuit that does not apply Logical Effort, with an improvement is about 44.15%. Meanwhile, the average improvement of CLA over RCA is about 64.85%, which means different circuit topologies would have different delays. The more complex a circuit is (high fan-in) it produces more delays. Gates number did not affected the delays in a circuit which sometimes, by having addition stages with same circuit function would improved the delays and produced fast response circuit.

TABLE OF CONTENTS

ACKNOWLEDGMENT	i
APPROVAL AND DECLARATION SHEET	ii
ABSTRAK	iii
ABSTRACT	iv
TABLE OF CONTENTS	v
LIST OF TABLES	vii
LIST OF FIGURES	viii
CHAPTER 1 INTRODUCTION	
1.1 Historical Background.....	1
1.2 Problem Statement.....	2
1.3 Project Scope.....	2
1.4 Impact, significance and contribution.....	3
1.5 Project Objectives.....	3
CHAPTER 2 LITERATURE REVIEW	
2.1 Logical Effort of a gate.....	4
2.2 Logical Effort of a circuit.....	8
2.3 Choosing best number of stages.....	9
2.4 Circuit Branches and Interconnect.....	11
2.5 Best Number of Stages.....	13
2.6 Carry Look-Ahead Adders.....	14

2.7	Logical Effort of Higher Valency Adders.....	18
2.8	Logical Effort using Particle Swarm Optimization Algorithm.....	19
2.9	Unified Logical Effort.....	21
2.10	Delay in a gate.....	21

CHAPTER 3 METHODOLOGY

3.1	Logical Effort equation and Flow Chart	23
3.2	Ripple-Carry Adder Schematic Design.....	25
3.3	Applying Logical Effort to Ripple-Carry Adder circuit.	26

CHAPTER 4 RESULTS AND DISCUSSION

4.1	4-bits Ripple-Carry-Adder (a) before sizing, (b) after sizing.....	32
4.2	Comparison of delays occurred in 4-bits Ripple-Carry-Adder and 4-bits Carry Look-Ahead Adder.....	34
4.3	Delay in Inverter.....	39

CHAPTER 5 CONCLUSION

5.1	Summary.....	42
5.2	Recommendation for future project.....	43
5.3	Commercialization Potential.....	43

REFERENCES.....45

- 1 Overview of Comparison of Delays Between 4-Bits Ripple-Carry Adder and 4-bits Carry Look-Ahead Adder Using Logical Effort Method.
- 2 Comparison of Delays Between 4-Bits Ripple-Carry Adder and 4-Bits Carry Look-Ahead Adder Using Logical Effort Method.

APPENDICES.....46

LIST OF TABLES

Tables No.		Page
2.1	Logical Effort of inverters, NAND, NOR and XOR gates [6].....	7
2.2	Parasitic delay of inverter, NAND and NOR, Tristate and Mux gates [6].....	8
2.3	Determination of stages number in order to be used for various path Effort.....	10
4.1	Comparison delays between before and after sizing 4-bits Ripple-Carry Adder circuit.....	35
4.2	Comparison delays between 4-bits Ripple-Carry Adder circuit with 4-bits Carry Look-Ahead Adder circuit.....	36

LIST OF FIGURES

Figures No.		Page
2.1	Inverter gate, NAND gate, NOR gate, and XOR gate [6].....	5
2.2	Information given only just the input capacitance and output Capacitance [6].....	8
2.3	After applying the Logical Effort method, all gate's sizes in a path can be calculate [10]	9
2.4	A path with different Logical and Electrical Efforts on each leg [6].....	11
2.5	Cases of adding 0, 1, 2, or 3 inverter [5].....	14
2.6	1-bit Partial Full Adder. [1].....	15
2.7	4-bit Ripple-Carry Adder [1].....	15
2.8	Carry Look-Ahead Adder [1].....	16
2.9	Logical Effort of Higher Valency Adders [3].....	18
3.0	Eight-stage Full Adder circuit [7].....	19
3.1	Flow chart to apply the Logical Effort method in RCA and development of CLA circuit.....	24
3.2	Schematic for 1bit Ripple-Carry Adder before sizing	25
3.3	Schematic for 4-bits Ripple-Carry Adder before sizing.....	25
3.4	1-bit Ripple-Carry Adder before sizing.....	26
3.5	1-bit Ripple-Carry Adder before sizing with some additional inverters.....	27

3.6	A part of 1 bit Ripple-Carry Adder that has branch.....	27
3.7	Second part of 1 bit Full Adder that has branch.....	29
3.8	NAND gate with ratio PMOS:NMOS = 3 : 2.....	30
3.9	Schematic design for Carry-Look-Ahead Adder.....	31
4.1	Waveform of 4bits Ripple-Carry-Adder before and after sizing.....	33
4.2	Comparison of delays occurred in 4bits Ripple Carry-Adder and 4bits Carry Look-Ahead Adder.....	34
4.3	Addition of two 4-bit numbers illustrating the generation of the carry-out bit.....	37
4.4	Ripple-carry adder, illustrating the delay of the carry bit.....	37
4.5	Block diagram of a 4-bits CLA.....	38
4.6	Inverter at PMOS and NMOS ratio 2:1.....	39
4.7	Inverter waveform at PMOS and NMOS ratio 3:1.....	40

© This item is protected by original copyright