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Effects of Series Resistance and Frequency on the Capacitance/ Conductance –Voltage C/G-V Characteristics of Au/GaN/GaAs and Au/GaAs Diodes

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ABSTRACT

In order to analyze the effect of the presence of the GaN layer and series resistance, the electrical characteristics of the Au/GaAsand Au/GaN/GaAsdiodes are investigated. The study is realized by a nitridation process of GaAs substrates. The GaN layer is growth in ultrahigh vacuum system with annealing operation realized at 620°C during one hour. (C-V) and (G-V) characteristics of Au/GaN/GaAs and Au/GaAs nanostructures at different frequencies have been studied. The estimated values of R_s showed a regular diminution. Since Rs causes errors in the extraction of electrical parameters. Consequently, the measured capacitance (C-V) and conductance (G-V) are corrected to obtain the real "corrected" capacitance (C_c-V) and (G_c-V) of the diodes. Thus, one showed clearly that the values of C_c and G_c increased proportionally with the applied bias voltage. This effect can be observed practically in the accumulation region and for a high frequency (1 MHz). From the C^{-2}-V curves and after correction, the diffusion potential V_d is evaluated to (0.32 V -0.25 V) and the potential barrier φ_{bn} is estimated equal to 0.38 eV and 0.31eV for Au/GaN/GaAs and Au/GaAs structures respectively. The states densities N_{ss} for Au /GaN/GaAs and Au/GaAs structures are determined at (E_c-0.2) with and without series resistances and are found equal to (7.3×10^{12} eV^{-1} cm^{-2} and 6.1×10^{10} eV^{-1} cm^{-2}) and (9.31×10^{10} eV^{-1} cm^{-2} and 10^{10} eV^{-1} cm^{-2}) respectively.

Keywords: GaN, GaAs, Nanostructures, Schottky Diodes, Nitridation.

1. INTRODUCTION

The nanostructures materials have received great attention due to their unique physical properties and especially those based on III-V and III-V nitrided materials.

GaN materials seem to be the most interesting designing electronic and optoelectronic devices such as LEDs and Laser diodes [1-2-3]. They are perfect candidates for manufacturing of high power microwave devices, breakdown field, frequency and high electron saturation velocity. They have applications in light emitters and detectors operating from the visible to UV spectral range [4-5]. However, growth of GaN presents a problem of substrates and disagreement of meshes with substrates resulting in lattice mismatch. Then, to obtain GaN thin films, one suggested to nitride GaAs substrates using a singular glow discharge source. This process has been later developed by deposing GaN monolayer or by exposing the GaAs substrate to an active nitrogen flow. This operation can also be used for the passivation and the stabilization of GaAs substrates [3-6].

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In this article, we propose the electrical study of Au/GaN/GaAs nanostructures. In order to study the effect of the presence of the GaN layer, these structures are compared to Au / GaAs structure. Current conduction mechanisms in these devices depend on different parameters, such as the series resistance R_s. In fact, this one plays an important role in the capacitance–bias voltage C–V and in conductance-bias voltage G–V characteristics [7–8]. Then, these parameters are corrected to obtain C_C-V and Gc-V characteristics.

Analysis of the electrical characteristics of the diodes only at one frequency using (C–V and G–V) measurements seems not to be sufficient to give large details on the conduction phenomena in the diodes. Thus, electrical measurements were realized at various frequencies providing information on conduction mechanisms and allowing the evaluation of physical and electronic parameters [9].

After that, series resistance effect on the parameters of the Au/GaN/GaAs and Au/GaAs diodes obtained from C-V and the G-V measurements such as doping concentration N_d, barrier height Φ_{bn} and the diffusion potential V_d are evaluated. Finally, interfacial states density N_{ss} are also investigated using the comparison between the C-V curves plotted at low (10 KHz) and high (1MHz) frequencies.

2. TECHNOLOGICAL PART

Used n-GaAs substrates are doped at 4.9×10^{15} cm^{-3}doping concentration and (100) orientation. The cleaning process of the substrates consists on many steps. First, substrates are cleaned in H_2SO_4 and deionized water successively. Then, they are treated with cold and hot methanol all combined with ultrasounds. Finally, substrates are dried by nitrogen N_2 flow.

To clean chemically the surface, substrates are bombarded using Ar^+ ion with sample current of 5 $\mu A/cm^2$ and ion energy of 1 keV. This operation is realized in UHV chamber at 6×10^{-5} Torr during one hour.

Nitridation operation is performed using a singular glow discharge source (GDS) [10]. Nitrogen cell produces continuous plasma at a power level of 5 W. Then, N atomic species are created at a nitrogen pressure of 10^{-4}Torr ion energy of 2.5 keV and a sample current of 1 $\mu A.cm^{-2}$. This operation is realized at the same UHV chamber at a temperature of 500°C during 30 min. The nitridation process is followed by an annealing treatment at temperature of 620°C during one hour.

To evaluate the chemical composition and crystal structure of the studied samples, we use an XPS system (dual anode Al-Mg X-ray source and hemispherical electron energy analyzer) presented in a home-built UHV chamber [11]. Then, GaN with thickness of2 nm is estimated by the comparison between experimental spectra and a theoretical model of the XPS peak intensity [11, 12].

On other hand and to study the effect of the GaN layer, we have realized another batch of structures without GaN film. The GaAs surface is cleaned in the same conditions.

Gold contact with thickness of 100 nm and surface equal to 4.41×10^{-4} cm^2 is deposited. To improve the quality of Ohmic contacts, Tin (Sn) is deposited on the back face using NH_4Cl at a temperature of 350 °C during 5 min. This process allowed diffusing Tin inside GaAs substrates [13].

Capacitance versus bias voltage C-V and conductance versus bias voltage G-V measurements are plotted at different frequencies (10 KHz, 100 KHz, and 500 KHz and 1 MHz) using Agilent 4294A Analyzer Impedance.

Figures 1a and 1b display the transversal cross section of the Au/GaN/GaAs and Au/GaAs diodes.

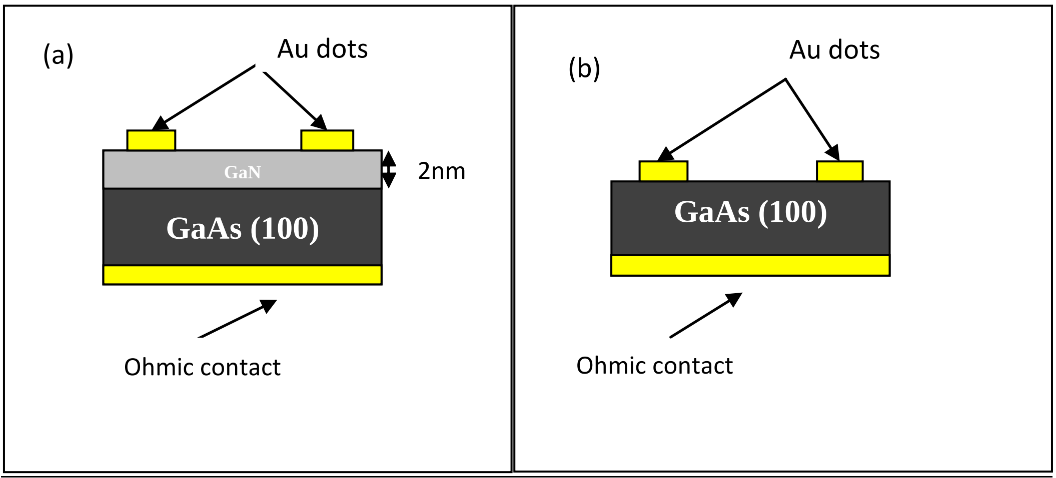

Figure 1. Transversal cross section of the Au/GaN/GaAs (a) and Au/GaAs (b) diodes.

3. RESULTS AND DISCUSSION

Capacitance C-V and conductance G-V versus bias voltage characteristics of the Au/GaN/GaAs and Au/GaAs diodes were plotted at different frequencies in the range of 10 KHz to 1 MHz and are given in figures 2 and 3, respectively.

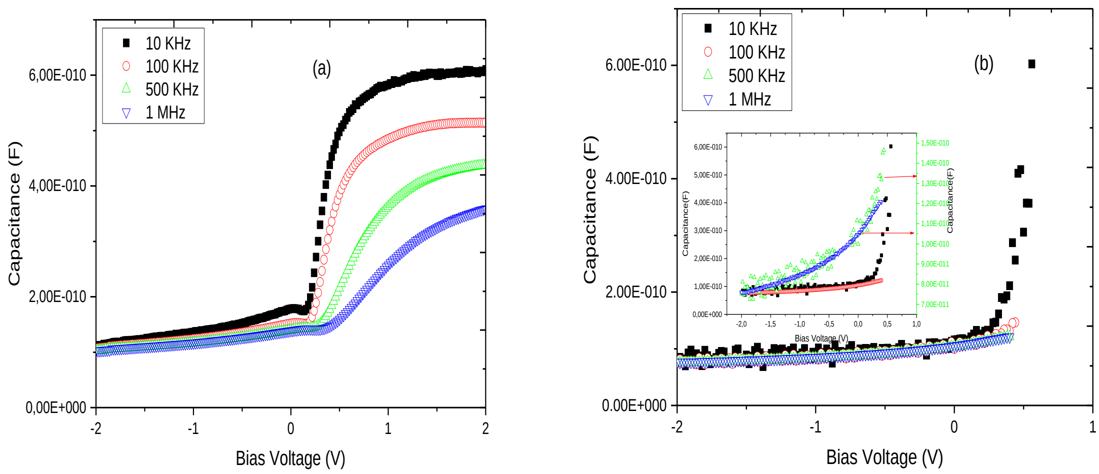

Figure 2. Capacitance–bias voltage characteristics of the Au/GaN/GaAs(a) and Au/GaAs (b) diodes plotted at different frequencies.

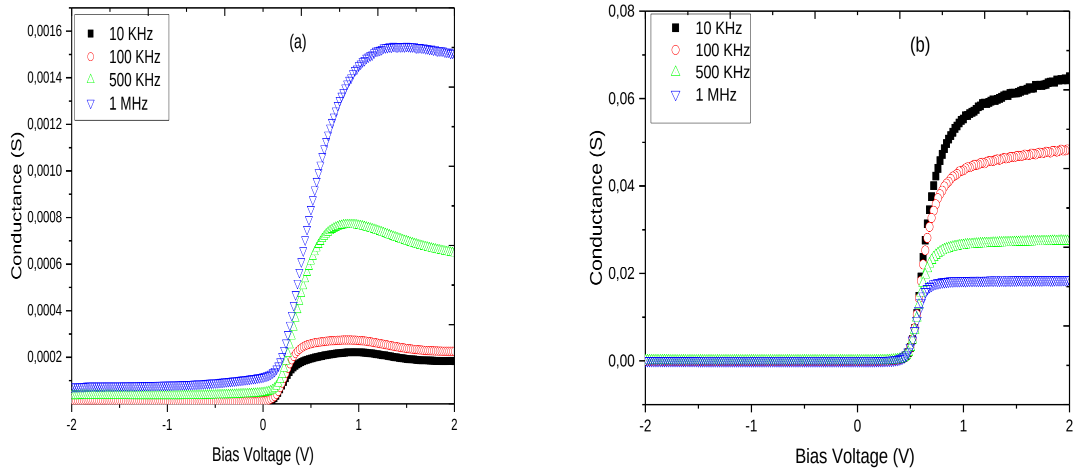

Figure 3. Conductance bias voltage characteristics of the Au/GaN/GaAs (a) and Au/GaAs(b) diodes plotted at different frequencies.

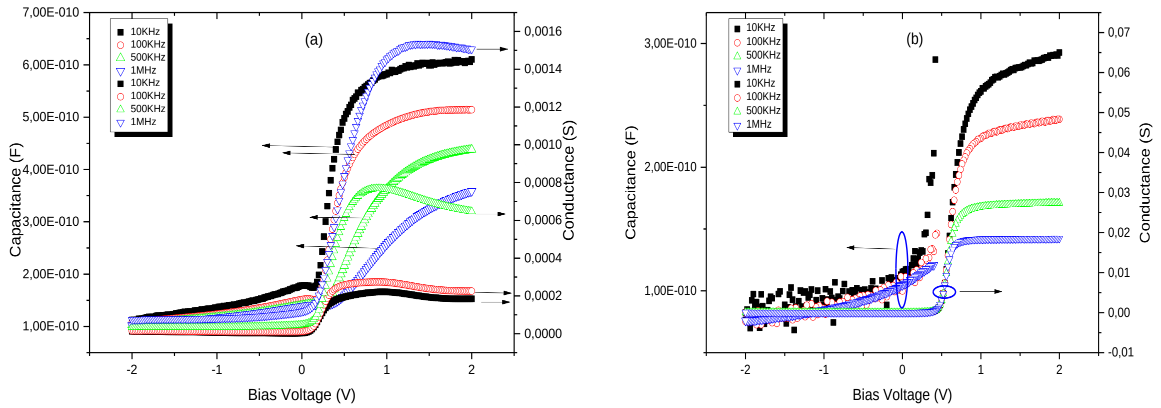

Figure 4. Conductance and Capacitance bias voltage characteristics of the Au/GaN/GaAs(a) and Au/GaAs (b) diodes plotted at different frequencies.

It appeared that the measured capacitance C_m and conductance G_m structures depend primarily on frequency and bias voltage. One can show that C–V plots indicated three regions similar to a specific MIS diode behavior. C-V plots showed a higher capacitance values at low frequencies. This excess capacitance can be expressed by the existence of interfacial states density N_{ss}. At a high frequency, N_{ss} cannot follow the a.c. signal and the contribution of these interface states to the total capacitance is insignificant. In another side and in the accumulation zone, a peak appears particularly for low frequencies. This can be explained by the presence of series resistance and ohmic back contact effects as shown in figure 5. These results are in good agreement with those obtained by Demirezen *et al.* and Tsormpatzoglou *et al.* [9, 14, 15].

Also, the conductance curves increased with decreasing of frequency, as shown in figure 3. This can be explained by the distribution of the interfacial states and traps which cannot follow the a.c signal more and more when the frequency increases.

The series resistance R_s is one of the most important electrical parameter which causes non-ideality in the C-V and G-V characteristics. Series resistance of Au/GaN/GaAs and Au/GaAs diodes can be estimated using the measured capacitance (C_m) and conductance (G_m) values in accumulation range at low frequency (f =10 KHz) [16].Then, R_s can be expressed as follow [17]:

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \quad (1)$$

where C_m and G_m are the measured capacitance and conductance versus bias voltage for each frequency and$\omega$is the angular pulsation and equal to $2\pi f$.

Using Equation(1), the values of R_s are calculated from figures 2 and 3 data as a function of bias voltage at several frequencies. The results are given in figure 5.

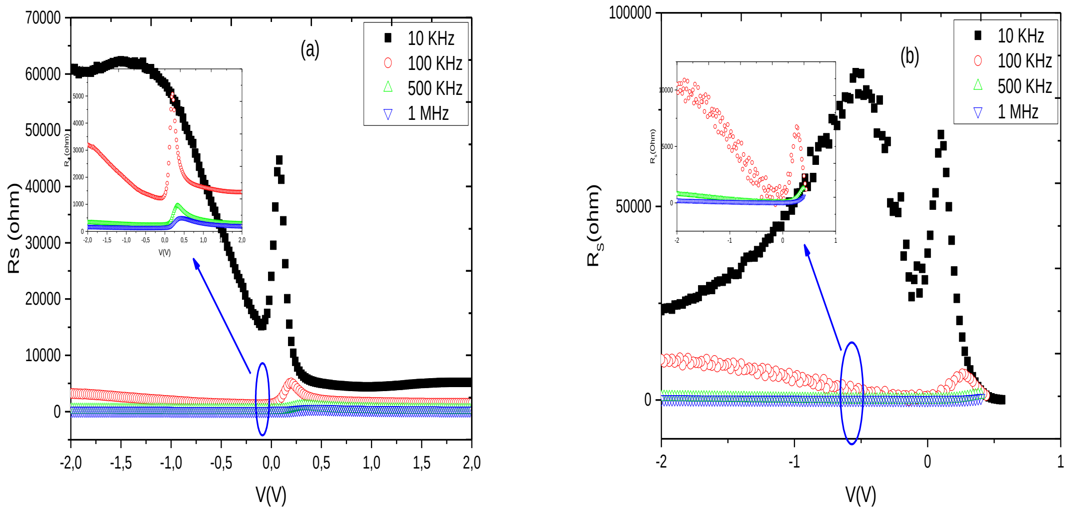

Figure 5. Series resistance versus applied bias voltage at different frequencies for Au/GaN/GaAs and Au/GaAs structures.

In figure 5a and at low frequency, one can observe an important peak of R_s at a bias voltage equal to 0.08 V. This can be attributed to the presence of interface states traps that, in this case, follow the modulation signal. In the other hand and in the Au/GaAs diodes (see figure 5b), we can observe two peaks (-0.54Vand 0.1V) at the low frequency (10KHz). These results are in a good agreement with those obtained by Demirezen *et al.* [9]. Indeed, they confirm the obtaining two peaks in the Au/GaAs diodes. They note that there are two peaks for Au/n-GaAs Schottky barrier diodes. This can be explained by the fact that one of the peaks is caused by the presence of N_{ss} and their particular distribution in semiconductor band gap and the other one is caused by the native interfacial layer.

On another hand and in the Au/GaN/GaAs structures, we have one peak only because the GaAs surfaces are been cleaned and therefore we have no oxide.

One can also observe, in the same figure, that when the frequency decreases the value of the peaks increases. This result is in a good agreement with that obtained by M. M. Bülbül *et al.* [18]. These have studied the effect of frequency on the capacitance and conductance–voltage characteristics of $Al/Si_3N_4/p\text{-}Si$ (100) MIS diodes.

Series resistance Rs versus applied bias voltage curves for Au/GaN/GaAs and Au/GaAs structures, shown in figure 5, present a very significant value of R_s. Series resistance influences greatly the electrical parameters of the diodes and presents an important values at low frequencies since one found resistance values of 44.7 KΩ, 5.06KΩ, 0.954 KΩ, 0.504KΩf or Au/GaN/GaAs and (80.508 KΩ- 68,582 KΩ),6.737 KΩ,1.302 KΩ,0.582 KΩ) for Au/GaAsat the range of frequencies going from 10KHz, 100KHz, 500KHz and 1MHz, respectively. Table 1 presents the position of the peaks and values of series resistances at different frequencies.

Table 1 Position of the peaks and values of series resistances at different frequencies

	Au/GaN/GaAs				**Au/GaAs**				
Frequencies	10 KHz	100 KHz	500 KHz	1 MHz	10 KHz		100 KHz	500 KHz	1MHz
Peak	0.08	0.2	0.32	0.44	-0.54	0.1	0.26	0.4	0.4
R_s (KΩ)	44.7	5.06	0.954	0.504	80.508	68.582	6.737	1.302	0.582

One also knows that the series resistance can induce an error in the determination of the electrical parameters at high frequencies [16, 19, 20]

To remove these errors, the capacitance C–V and conductance G–V characteristics at 1MHz are corrected using the following equations [16]:

$$C_c = \frac{[G_m^2+(\omega C_m)^2]C_m}{a^2+(\omega C_m)^2} \tag{2}$$

And

$$G_c = \frac{G_m^2+(\omega C_m)^2 a}{a^2+(\omega C_m)^2} \tag{3}$$

where G_c and C_c are the corrected conductance and capacitance, respectively

Parameter a is given by the following equation:

$$a = C_m - [G_m^2 + (\omega C_m)^2]R_s \tag{4}$$

The C_c-V and G_c-V characteristics of the Au/GaN/GaAs and Au/GaAs diodes are plotted at 1 MHz and are given in figures 6 and 7, respectively.

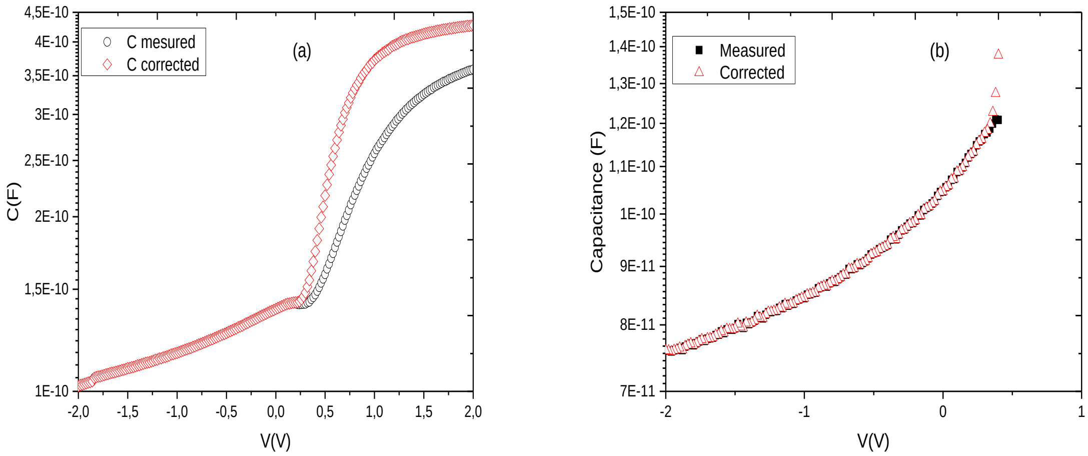

Figure 6. Corrected and measured capacitances versus bias voltage of the Au/GaN/GaAs (a) and Au/GaAs (b) diodes plotted at 1 MHz.

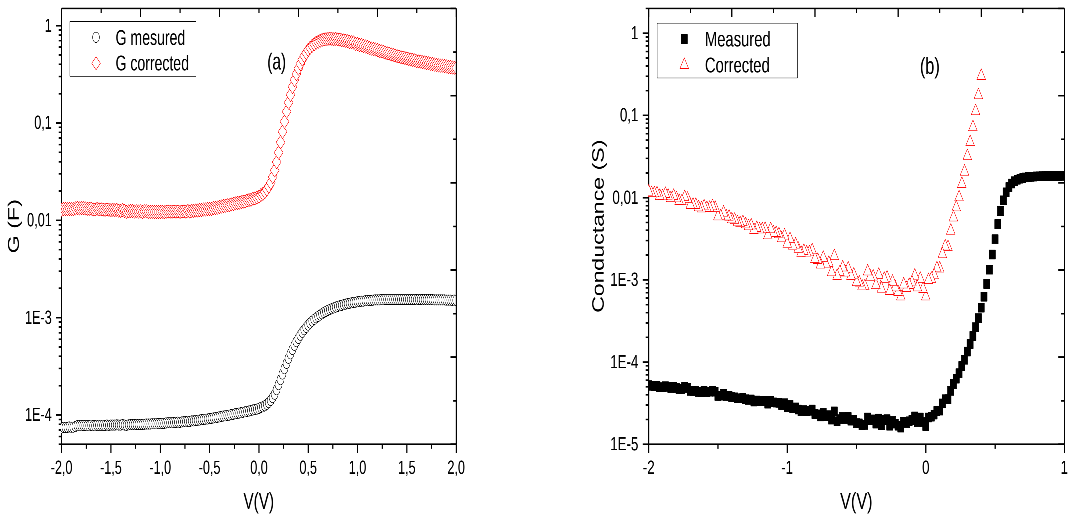

Figure 7. Measured conductance-bias voltage G-V and corrected conductance-bias voltage G_c-V curves of the Au/GaN/GaAs diode plotted at 1MHz high frequency.

After correction, one can see that the value of the C_c is confused with C_m in the interval [-2V, 0.32V] and from 0.32 V both curves begin to move away. In the other side G_c increases in all range with applied voltage. We're assisting to a translation of both curves. Corrected C_c showed an important increase with bias voltage in both depletion and accumulation regions. It's clearly observed that both change in C-V and G-V characteristics can be affected by R_s. So R_s caused errors in the evaluation of the electrical parameters.

Figure 8 shows capacitance–voltage ($1/C^2$–V) characteristics of Au/GaN/GaAs and Au/GaAs diodes at 1MHz.

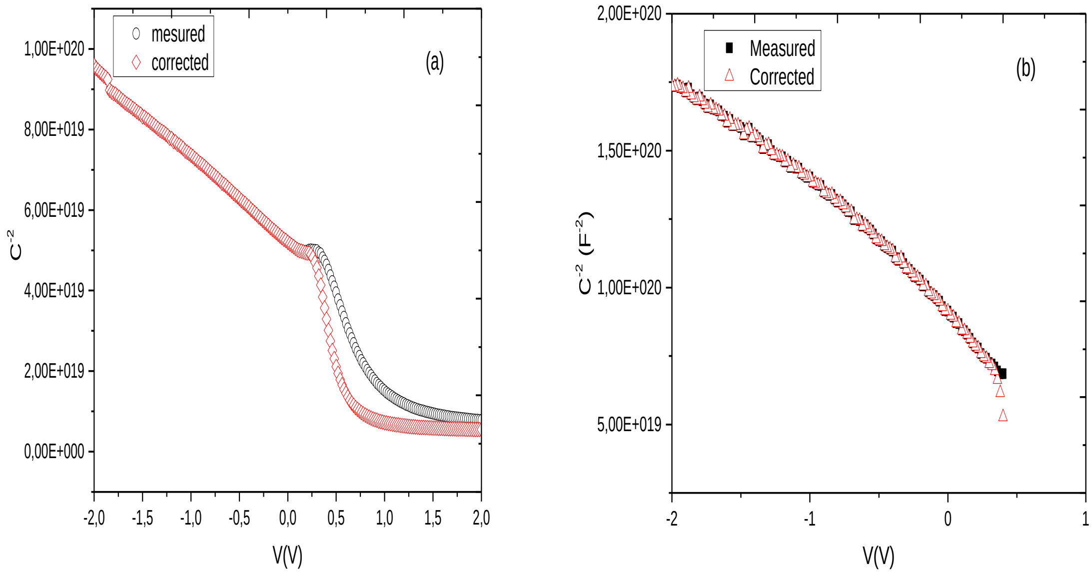

Figure 8. Measured and corrected C^{-2}-V plots of the Au/GaN/GaAs and Au/GaAs diodes at 1MHz.

Electrical parameters of the Au/GaN/GaAs and Au/GaAs, such as the diffusion potential V_d and the barrier height Φ_b are evaluated using C^{-2}-V curves. Diffusion potential is obtained by the extrapolation of the linear region of the C^{-2}-V characteristic and is found equal to 0.32 eV and 0.25 eV for Au/GaN/GaAs and Au/GaAs structures respectively. The barrier height $\Phi_b$is given by [16]:

$$\Phi_b = V_d + \frac{kT}{q} ln \frac{N_C}{N_d} \quad (5)$$

where T, k, N_c are the room temperature, the Boltzmann constant and effective concentration of electrons respectively.

Then, one can deduce the barrier height Φ_b and found a value of 0.38eVfor Au/GaN/GaAs diode and0.31eV for Au/GaAs diode. Doping concentration can be calculated from the slope of the linear region of the C^{-2}-V characteristic using the following equation [21]:

$$\frac{dC^{-2}}{dV} = \frac{2}{q\varepsilon_S S^2 N_d} \quad (6)$$

where ε_s is the substrate permittivity and S the area of the metallic gate (Au).

The value of the concentration doping is then found equal to 3.49×10^{16} cm^{-3} and 10^{16} cm^{-3} for Au/GaN/GaAs and Au/GaAs structures respectively. These two values are slightly higher than that of the GaAs substrate; this can be due probably to the oxygen present in the enclosure.

Electrical parameters of the Au/GaN/GaAs and Au/GaAs diodes extracted from the corrected C-V characteristics are summarized in table 2.

Table 2 The electrical parameters of the Au/GaN/GaAs and Au/GaAs diodes obtained using C^{-2}-V curves

Au/GaN/GaAs			Au/GaAs		
V_d (V)	N_d (cm^{-3})	Φ_b (eV)	V_d (V)	N_d (cm^{-3})	Φ_b (eV)
0.32	3.49×10^{16}	0.38	0.25	2.79×10^{16}	0.31

The other parameter still having influence on both C and G measurements is the interface states and particular distribution in the semiconductor band gap. The figure 9 presents the equivalent circuit of Au/GaN/GaAs diode.

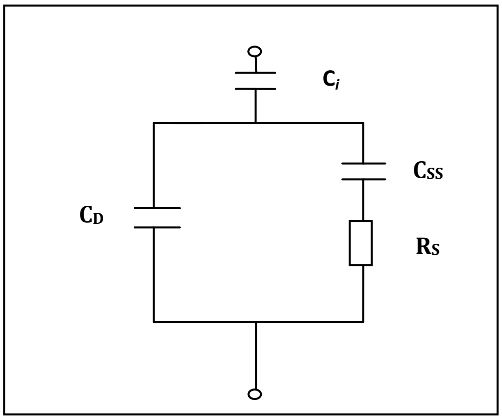

Figure 9. The equivalent circuit of Au/GaN/GaAs diode [17-21].

Where C_D,C_i, C_{SS} and R_S are the capacitance of space charge area, the capacitance of the interfacial layer, the capacitance due to interface states and the series resistance, respectively.

Interfacial states density N_{ss} can be evaluated by the C-V characteristics using the comparison between the high and low frequencies method with and without the effect of the series resistance [16]. Interfacial states capacitance C_{ss} can be extracted by subtracting the depletion layer capacitance determined from the measured high frequency capacitance C_{HF}, from the depletion layer capacitance in parallel with interfacial states capacitance determined from the measured low frequency capacitance C_{LF}.

Interfacial states density is calculated using the following relation:

$$qSN_{ss} = C_{ss} = \left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_i}\right]^{-1} \quad (7)$$

C_i is the capacitance of interfacial layer and it can be obtained from C–V and G–V measurements using the following relation [16]:

$$C_i = C_m\left(1 + \frac{G_m^2}{\omega C_m^2}\right) \quad (8)$$

Figure 10 shows interfacial density energy distribution in the band gap of Au/GaN/GaAs and Au/GaAs diodes.

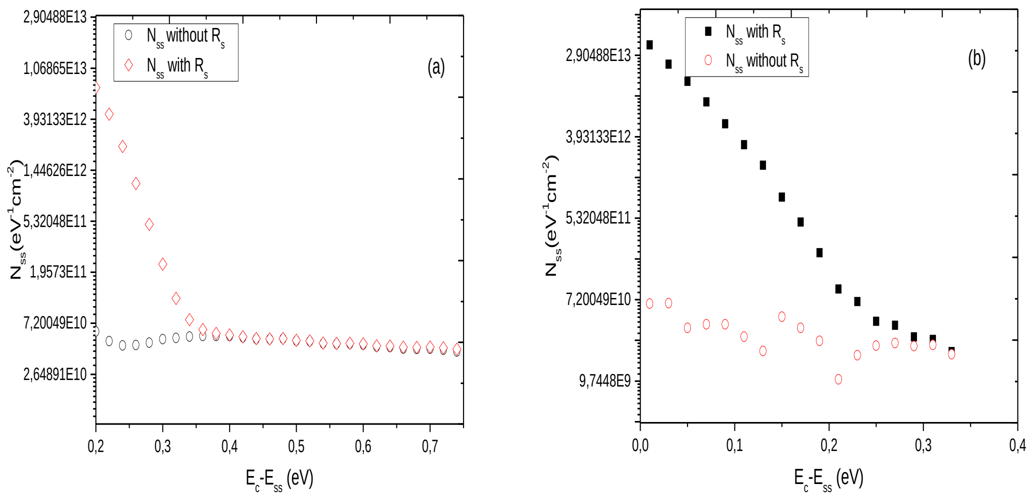

Figure 10. Interfacial states density distribution in the band gap of Au/GaN/GaAs (a) and Au/GaAs(b)diode with and without series resistance.

N_{ss} values calculated by elimination of the series resistance R_s are lower than those calculated with R_s. One can deduce the value of the interfacial states density distribution N_{ss} equal to $7.3 \times 10^{12} eV^{-1} cm^{-2}$at ($E_c$-0.2)eV and $6.1 \times 10^{10} eV^{-1}$ cm^{-2}withand without series resistance respectively for Au/GaN/GaAs.

The states density is also evaluated for Au/GaAs diode at (E_c-0.2) and is equal to $9.31 \times 10^{10} eV^{-1}$ $cm^{-2}$and $10^{10} eV^{-1}$ $cm^{-2}$with and without series resistance respectively .In the middle of the band gap, N_{ss} is the same in both cases and it is equal to $4.5 \times 10^{10} eV^{-1}$ cm^{-2}at (E_c-0.65)eV.

We show clearly, in both cases, that the states density decreases when the electrical characteristics are corrected and consequently, the performance of devices is improved.

4. CONCLUSION

C-V and G–V characteristics of Au/GaN/GaAs nanostructures and Au/GaAs diodes are studied at room temperature for (-2V)-(+2V) bias voltage at different frequencies (10KHz, 100KHz, 500KHz and 1MHz).

In order to obtain correct parameters values, the C-V and G-V curves are corrected by eliminating the series resistance effect which is particularly induced by back ohmic contacts and resistivity of substrate. Results show an improvement of the electrical parameters of the Au/n-GaN/GaAs and Au/GaAs diodes. After correction and using the C^{-2}-V curves, the diffusion potential V_d and the potential barrier φ_{bn} are evaluated equal to 0.32V and 0.38 eV for the Au/GaN/GaAs and 0.25V and 0.31eV for the Au/GaAs diodes respectively.

The exploitation of capacitance and conductance characteristics mainly depending on the bias voltage and frequency allows the calculation of interfacial states densities N_{ss} with and without series resistance. N_{ss} is determined at (E_c-0.2) and is equal to 6.1×10^{10} eV^{-1} $cm^{-2}$for the Au/GaN/GaAs and 10^{10} eV^{-1} $cm^{-2}$for Au/GaAs diodes respectively. Then, we conclude that when the capacitance and conductance are corrected, the results of electrical parameters are improved.

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