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FABRICATION AND CHARACTERIZATION OF ULTRA THIN SiO_2 FOR NANO DEVICES: SURFACE MORPHOLOGY AND ELECTRICAL STUDY

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By

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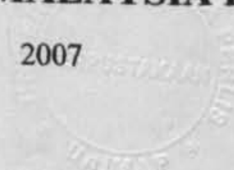

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TABLE OF CONTENTS

		Page
PERMISSION TO USE		i
ACKNOWLEDGEMENTS		ii
TABLE OF CONTENTS		iii
LIST OF TABLES		viii
LIST OF FIGURES		ix
ABBREVIATIONS		xiii
ABSTRAK		xv
ABSTRACT		xvi
CHAPTER 1	**BACKGROUND**	
1.1	Introduction	1
1.2	Research Objectives	4
1.3	Problem Statements	5
1.4	Research Scope	5
1.5	Thesis Overview	5
CHAPTER 2	**LITERATURE REVIEW**	
2.1	Introduction	7
2.2	Silicon dioxide	7
2.2.1	Silicon dioxide structure	8
2.2.2	Silicon Dioxide as a Device Dielectric	9

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2.3	Thin oxide	10
2.3.1	Growth Techniques	10
2.3.2	Growth Mechanism and Kinetics	11
2.3.3	Factors Affecting Oxidation Rates	16
2.3.3.1	Orientation Dependence of Oxidation Rates	16
2.3.3.2	Influence of Dopants	17
2.3.3.3	Effects of Halogens	17
2.3.3.4	Effects of Pressure	17
2.4	MOS Capacitors	18
2.4.1	The Si/SiO_2 interface and Oxide traps	18
2.4.1.1	Interface Trap Charge, Q_{it}	19
2.4.1.2	Fixed Oxide Charge, Q_f	20
2.4.1.3	Mobile Ionic Charge, Q_m	21
2.4.1.4	Oxide Trap Charge, Q_{ot},	22
2.4.2	MOS Capacitance Voltage Measurements	23
2.4.2.1	Accumulation region	24
2.4.2.2	Depletion region	24
2.4.2.3	Inversion region	25
2.4.2.4	Energy band diagram	26
2.4.2.5	Flatband diagram	27
2.4.3	Oxide Breakdown	28
2.5	Fabrication Process	30
2.5.1	Silicon Wafers	31
2.5.2	Cleaning Process	31
2.5.3	Oxidation	32
2.5.4	Photolithography	32

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2.6	Surface Morphology Characterization	33
2.6.1	Thickness measurement	33
2.6.1.1	Film Thickness Instrument	34
2.6.1.2	Extracting Oxide Thickness through capacitance Measurement	36
2.6.1.3	Color chart	36
2.6.2	Surface roughness	38
2.7	Electrical Characteristic	38
2.7.1	Capacitance-Voltage Characteristic	38
2.7.2	Current-Voltage Characteristic	41
2.7.3	Resistance and Resistivity	42
CHAPTER 3	**METHODOLOGY**	
3.1	Introduction	44
3.2	Equipment and consumable	44
3.2.1	Equipment	44
3.2.1.1	High temperature Furnace	44
3.2.1.2	Ellipsometer	45
3.2.1.3	Metal Evaporator	46
3.2.1.4	Atomic Force Microscopy (AFM)	48
3.2.1.5	Scanning Electron Microscope	50
3.2.1.6	Four Point Probe	52
3.2.1.7	CV System	54
3.2.1.8	IV System	55
3.2.2	Consumable	57
3.2.2.1	RCA Solution	57

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3.2.2.2	Positive Photoresist	57
3.2.2.3	Aluminum etchants	58
3.3	Experimental Setup	59
3.3.1	Wafer preparation	59
3.3.2	Oxidation	59
3.3.3	Metallization	62
3.3.4	Photolithography	63
3.3.5	Aluminum etching	65
3.3.6	Surface Morphological Characterization	67
3.3.6.1	Thickness measurement	67
3.3.6.2	Surface Topography	69
3.3.7	Electrical characterization	69
3.3.7.1	Capacitance Voltage Measurement	69
3.3.7.2	Current Voltage Measurement	70

CHAPTER 4 RESULTS AND DISCUSSIONS

4.1	Introduction	71
4.2	Surface Morphological Characteristic	72
4.2.1	Simulation	72
4.2.2	Statistical Design	74
4.2.3	Refractive Index	82
4.2.4	Surface Characteristic	83
4.3	Electrical Characteristic	91
4.3.1	Sheet Resistance	91
4.3.2	Capacitance-Voltage Characteristic	93

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4.3.3 Current-Voltage Characteristic 99

CHAPTER 5 CONCLUSION

5.1 Introduction 105

5.2 Conclusion 105

5.3 Suggestion 108

5.3.1 Oxynitride 109

REFERENCES **111**

APPENDICES A: RESEARCH PROPOSAL **118**

APPENDICES B: TABLES AND FIGURES **134**

APPENDICES C: LIST OF PAPERS **139**

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LIST OF TABLES

Table

2.1	Variation in parabolic and linear rate constants with temperature and orientation during oxidation of silicon dioxide	16
2.2	Silicon dioxide thickness colour chart	37
3.1	Oxidation process parameters	61
4.1	Experimental parameters arranged in Taguchi's orthogonal array	75
4.2	Silicon dioxide thickness obtain using ellipsometer	75
4.3	The S/N ratio for each wafer	76
5.1	Alternative high-k dielectric	108

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LIST OF FIGURES

Figure

1.1 Experimental growth of the number of components per MOS IC chip 2

1.2 Historical trends in thickness of SiO_2 uses as gate insulator in CMOS logic vs. year of publication 4

2.1 Growth of SiO_2 8

2.2 Schematic showing a SiO_4 tetrahedron. The mean value of Si-O-Si angle is 153^0 in vitreous silica. The Si atom has a hybrid sp^3 configuration, and the oxygen atom has a p^4 configuration, there is thus one unpaired electron on each oxygen atom. The structural formula is often represented as SiO^{4-}_4 9

2.3 A thin layer of silicon dioxide is grown in the gate region 10

2.4 Basic model for thermal oxidation of silicon. 12

2.5 MOS capacitance structure 18

2.6 Schematically shows these charges in oxidized silicon 19

2.7 High frequency CV curve showing the effect of the presence of oxide charge 22

2.8 Charges in a Metal-Oxide-Semiconductor structure under accumulation, depletion and inversion conditions 23

2.9 Energy band diagram of an MOS structure biased in inversion. 27

2.10 Flatband energy diagram of a metal-oxide-semiconductor (MOS) structure consisting of an aluminum metal, silicon dioxide and silicon 28

2.11 A schematic of the wearout/breakdown process showing trap generation and the formation of breakdown paths 30

2.12 C-V curve example for p-type MOS capacitor 40

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2.13	Example of Gate current density J_G as a function of oxide voltage V_{ox} of an MOS capacitor with a 4.2 nm gate oxide layer stressed under a constant voltage $V_G = 5$ V. The J_G - V_{ox} characteristics were measured after different time stress t	41
2.14	Relationship of resistance to resistivity and dimensions	43
3.1	High Temperature Furnaces	45
3.2	Ellipsometer	46
3.3	Physical Vapor Deposition	47
3.4	A schematic of thermal evaporator PVD	48
3.5	Atomic Force Microscopes	49
3.6	AFM sensitivity is in the 1Å range and can be operated in contact or noncontact modes	49
3.7	AFM schematic	50
3.8	Scanning Electron Microscope	51
3.9	Four Point Probe systems	53
3.10	Four-point probe measurement of thin layer	53
3.11	Keithley 595 and CV system	54
3.12	CV probe station	55
3.13	Keitley 4200 SCS	56
3.14	Probe station	56
3.15	Positive photoresist	58
3.16	Step by step process of wafer preparation	59
3.17	Loading wafers into the furnace.	60
3.18	Step by step process of dry oxidation using a high temperature furnace	61
3.19	Process sequence summary of metallization	62
3.20	Actual design using AutoCAD	64

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3.21 Process sequence summary of metallization 65

3.22 Etching process 66

3.23 Actual wafer pattern capture using SEM 66

3.24 Measurement points 68

3.25 Process sequence summary of thickness measurement 69

4.1 Oxide thickness result obtain using TCAD simulation 73

4.2 Factor affecting the oxide growth 77

4.3 Silicon dioxide thickness obtained from Taguchi's method Calculation 79

4.4 Oxide grown at 800^0C at 3 minutes at different oxygen flow rates 81

4.5 The reflective index of silicon dioxides results obtained using ellipsometer 82

4.6 (a) Topography image of $100nm^2$ oxide surface 83

4.6 (b) Cross section of oxide surface 84

4.6 (c) Peak distribution of oxide 84

4.7 (a) Topography image of $100nm^2$ oxide surface 85

4.7 (b) Cross section of oxide surface 86

4.7 (c) Peak distribution of oxide 86

4.8 (a) Topography image of $100nm^2$ oxide surface 87

4.8 (b) Cross section of oxide surface 88

4.8 (c) Peak distribution of oxide 88

4.9 RMS value for wafer 1, 2 and 3 89

4.10 SEM image of a surface of silicon dioxide and bare wafer 90

4.11 Sheet resistance 92

4.12 Ideal and experimental C-V curve of a 1.88nm silicon dioxide capacitor with an area of $0.0471cm^2$ measured at 1 MHz frequency 93

4.13 Voltage versus time characteristics for wafer 1 94

4.14 Ideal and experimental C-V curve of a 2.67nm silicon dioxide capacitor with 95

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an area of $0.0616 cm^2$ measured at 1 MHz frequency

4.15 Voltage versus time characteristics for wafer 2 96

4.16 Ideal and experimental C-V curve of a 2.80nm silicon dioxide capacitor with an area of $0.0380 cm^2$ measured at 1 MHz frequency 97

4.17 Voltage versus time characteristics for wafer 3 98

4.18 Gate current density J_G versus oxide voltage V_{ox} of a 1.8 nm gate oxide layer recorded at different times after constant voltage stress $V_G = +0.2$ V 100

4.19 Gate current density J_G versus oxide voltage V_{ox} of a 2.67 nm gate oxide layer recorded at different times after constant voltage stress $V_G = +0.2$ V 101

4.20 Gate current density J_G versus oxide voltage V_{ox} of a 2.8 nm gate oxide layer recorded at different times after constant voltage stress $V_G = +0.2$ V 102

4.21 Fowler-Nordheim tunneling current density through silicon dioxide as function of applied field 103

5.1 Reactions to form nitride layer in the dielectric 110

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ABBREVIATIONS

Symbol	Description	Unit
A	Area	
Å	Angstrom	
AFM	Atomic Force Microscope	
B	Boron	
C	Capacitance	
CV	Capacitance-Voltage	
C_{ox}	Oxide Capacitance	pF
°C	Celsius	
ε_{ox}	dielectric constant of the SiO_2	F/cm
ε_o	permittivity of the free space	F/cm
HFCV	High Frequency CV	
I	Current	
IV	Current-Voltage	
J_G	Gate Current Density	
MOS	Metal-Oxide-Semiconductor	
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistors	
Neff	effective oxide charge concentration	unit/cm^3
Ph	Phosphorus	
q	Electron charge	C
Q_{it}	Interface trap charge	Coul/cm^2
Q_f	Fixed oxide charge	Coul/cm^2
Q_m	Mobile ionic charge	Coul/cm^2
Q_{ot}	Bulk oxide trapped charge	Coul/cm^2
Q_{eff}	effective oxide charge	Coul/cm^2

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RMS	Root Mean Square	
Rs	Sheet Resistance	
SEM	Scanning Electron Microscope	
Si	Silicon	
SILC	Stress Induce Leakage Current	
SiO_2	Silicon Dioxide	
S/N	Signal to Noise	
t_o	oxide thickness	nm
ULSI	Ultra-large-scale integrated	
V	Volt	
VLSI	Very-Large-scale integrated	
V_{FB}	Flat Band Voltage	Volt
V_T	Threshold Voltage	Volt
V_G	Gate Voltage	Volt
Ω	Ohm	
ρ	Resistivity of Wafer	
Φ	Metal Work Function	

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ABSTRAK

Tujuan penyelidikan ini adalah untuk memfabrikasi dan mencirikan (elektrikal dan optikal) filem nipis silikon dioksida untuk kegunaan peranti pada saiz nano meter. Dalam penyelidikan ini, proses pengoksidaan kering menggunakan relau bersuhu tinggi digunakan untuk menghasilkan filem nipis oksida. Ketebalan filem nipis ini perlu dibawah 30 Angstroms untuk dijadikan penebat didalam peranti kapasitor MOS. Terdapat tiga takat suhu yang digunakan, iaitu 750, 800 and 850^{0}C. Sampel disediakankan pada pengaliran oksigen 0.333 litre/min, 0.667 liter/min and 1.00 liter/min dan dengan perubahan masa iaitu 1, 2 and 3 minit. Ketebalan diukur menggunakan ellipsometer dan sifat permukaan mikro dan topografi diperolehi menggunakan alat *atomic force microscope* (AFM). Semua parameter dan data telah di interpritasikan menggunakan teknik Taguchi untuk menganalisa faktor-faktor penting dalam penghasilan filem nipis silikon ini. Melalui pengiraan, teknik Taguchi boleh digunakan untuk meramal ketebalan untuk setiap kombinasi parameter yang digunakan. Keputusan menunjukkan suhu merupakan faktor terpenting yang mempengaruhi pertumbuhan oksida. Keputusan juga menunjukkan pengaliran oksigen juga mempengaruhi ketebalan dan ciri permukaan oksida. Pada pengaliran oksigen yang tinggi (1 l/min), ketebalan oksida akan meningkat dan pada masa yang sama permukaan akan menjadi halus. Terdapat juga keputusan CV berfrekuensi tinggi dan IV yang telah dijalankan untuk mengkaji sifat elektrikal peranti tersebut. Keputusan CV menunjukkan terdapatnye perubahan pada voltan jalur lebar (V_{FB}) pada ketiga-tiga sampel. Keputusan IV pula menunjukkan kegagalan berlaku pada paras yang lebih rendah iaitu 1MV/cm.

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ABSTRACT

The aim of this research is to fabricate and characterize (optical and electrical) an ultra thin silicon dioxide for sub nano devices. In this research, dry oxidation method using high temperature furnace is chosen to fabricate a thin layer of oxide below 30Angstroms. There are three level of temperature used, that is 750, 800 and 850^{0}C. The wafers were grown in 0.333 litre/min, 0.667 liter/min and 1.00 liter/min oxygen flow rate with variation in growth time 1, 2 and 3 minutes. Thicknesses were obtained using ellipsometer and the surface topography and were achieved using atomic force microscope (AFM). Parameters and data has been interpreted using Taguchi's method. This is to analyze the most affecting factors in producing an ultra thin silicon dioxide. Taguchi's method were able to predict the thickness for each combination of parameters. Results show that the temperature is the most effecting factor that effects the growth of oxide. Results also show that oxygen flow rates do have an influence to the thickness and surface properties. A higher amount of flow rate (1 l/min) will increase the oxide thickness and also will create a smooth oxide surface. There are also results of a high frequency CV and IV techniques were employed as for the devices electrical characterizations. The CV results shows that there is a shift in V_{FB} for all the wafers and IV shows that breakdown occurs at 1 MV/cm.

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CHAPTER 1

BACKGROUND

1.1 Introduction

The electronics industry has grown rapidly in the past three decades. Ultra-large-scale integrated (ULSI) circuits, with 10^8 or more devices on a chip, can now be fabricated on semiconductor substrates, or wafers, to reduce cost and to increase the performance of electronic products. Figure 1.1 shows the growth of the number of components on a metal-oxide-semiconductor (MOS) memory chip. This number has approximately doubled every two years over the past two decades, matching the rate Moore forecast [Mur, 2001]. Concurrently, the minimum dimension of the device-feature continues to shrink by about 13% per year, or by a factor of two every six years, due to the advances in fabrication technology. The decrease of feature length reduces the overall device size and increases the packing density, and thus reduces the cost of function. Moreover, device speed, which varies inversely to feature length, has been improved and power consumption, which approximately varies as the square of feature length, has been reduced. On the other hand, the complexity of microchip design and fabrication has increased continuously with integration and miniaturization [Rusu, 2001].

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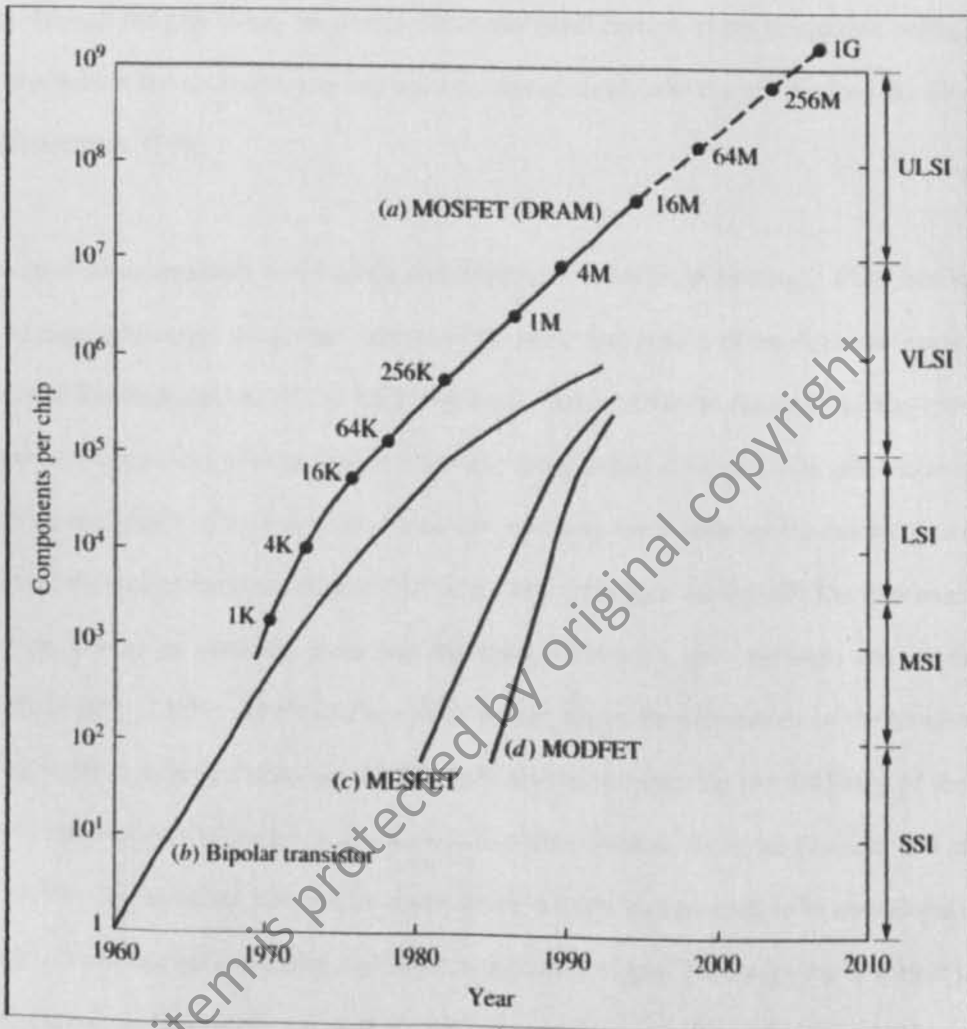

Figure 1.1: Experimental growth of the number of components per MOS IC chip [Intel, 2002]

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Integrated circuitry based on metal-oxide-semiconductor field effect transistors (MOSFETs) is the dominant technology in the semiconductor industry. At the heart of each of these transistors is a gate that controls the flow of electrons through a channel between a source and a drain. The name field effect refers to the control of the conductivity within the channel caused by the presence of an electric field. Between the gate and the channel is a very thin dielectric, creating capacitor effect. Generally, this dielectric is a thermal oxide grown directly on the silicon wafer. This oxide film, known as the gate oxide, is critical to the proper functioning of the FET transistor. If there is

leakage through the gate oxide, the device draws too much current. If the breakdown voltage is too small, the field in the channel is too low and one cannot control the current between the source and drain [Hasunuma, 1999].

In advanced complementary metal-oxide-semiconductor (CMOS) technology, while moving from micro to nanotechnology, the precise control of thickness and quality of the different layers grown, are decisive for the behaviour of the MOS transistor. One of the main issues in microelectronics is the growth of ultra-thin oxide on silicon substrates [Sze, 1988]. The ultra-thin gate oxide is a thin layer of oxide (usually silicon dioxide) forms the insulating layer between the control gate and the conducting channel of the transistors, which turns the current flow on and off. The gate oxide layer, in essence, acts as an insulator, protecting the channel from the gate electrode and preventing a short circuit [May, 2004]. As circuits are made denser, all of the dimensions of the transistors are reducing correspondingly [Mahajan, 1999]; these also mean reducing the thickness of the oxide. However reducing the thickness is not an easy solution because there are physical and practical limits on how thin an oxide film can be made. There are also factors need to be considered such as reliability, direct current tunnelling and oxide breakdown. Figure 1.2 shows the historical trend in oxide thickness for high-performance logic applications over the past decade [Sze, 1988].

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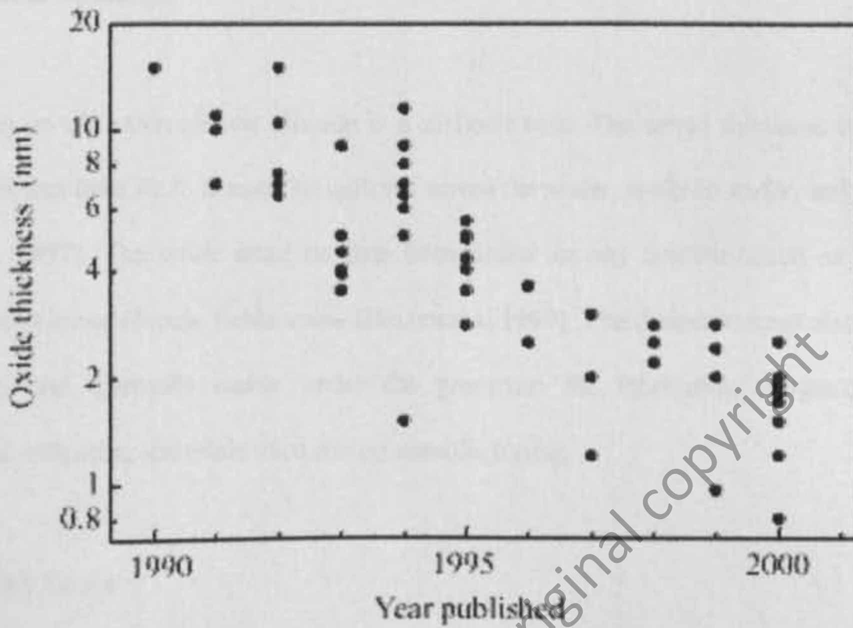

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Figure 1.2: Historical trends in thickness of SiO_2 uses as gate insulator in CMOS logic vs. year of publication [Sze, 1988].

Achieving reliable and high quality thin gate dielectrics requires research and development efforts to meet the demands for smaller device geometry and better device performance [Campbell, 2001].

1.2 Research Objectives

The goal of this project is to fabricate, characterize and optimize electrical and surface morphology of ultra-thin silicon gate oxide and alternate gate dielectrics for sub 0.1μm Metal Oxide Semiconductor (MOS) devices.

1.3 Problems Statement

Fabricating an ultra-thin silicon dioxide is a difficult task. The target thickness to be considered ultra thin is less than 30 Å. It must be uniform across the wafer, wafer to wafer, and from run to run [Momose, 1997]. The oxide must be free from defect or any contamination as it would cause breakdown at lower electric fields value [Hasunuma, 1999]. The dielectric must also be chemically, electrically and thermally stable under the processes for fabricating integrated circuits and compatible with other materials used during manufacturing.

1.4 Research Scope

The main focus of this research is to be able to fabricate ultra-thin silicon dioxide. This research consists of simulation, design of experiment for fabricating thin oxide using high temperature furnace. It include characteristic of silicon oxide such as surface properties, growth rate, topography, roughness and refractive index. It also involves in electrical characteristic such as resistivity, capacitance-voltage and current voltage results.

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1.5 Thesis Overview

In chapter 1, it consists of an introduction to the CMOS technology and history trends. It explains on why the thin oxide is needed for future technologies. In this chapter, it also describe in detail about problem statement, research objectives and the research scope.

Chapter 2 describe about literature review on silicon dioxide, the structure, the growth techniques, factors affecting the oxide and theoretical of MOS capacitors. It also describes the basic of fabrication process and measurement process.

Chapter 3, describe in detail about the research methodology. It shows the approach used to fabricate and characterize an ultra thin silicon dioxide in CMOS capacitor.

Chapter 4 discuss about the result achieved. This include the surface characteristic such as oxide thicknesses obtain by TCAD simulation and by Taguchi's statistical design, the surface roughness and the electrical characteristic which is the capacitance voltage and current voltage measurement.

Chapter 5 presents conclusion of this research and a list of possible direction for future research.

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CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The oxidation of silicon is necessary throughout the modern integrated circuit fabrication process. Producing high-quality ICs requires not only an understanding of basic oxidation mechanism, but the ability to form a high-quality oxide in a controlled and repeatable manner. In addition, to ensure the reliability of the ICs, the electrical properties of the oxide must be understood [CSEE, 2007].

Silicon dioxide has several uses: to serve as a mask against implant or diffusion of dopant into silicon, to provide surface passivity, to isolate one device from another (dielectric isolation as opposed to junction isolation), to act as a component in MOS structures, and to provide electrical isolation of multilevel metallization systems. Several techniques for forming the oxide layers have been developed, such as thermal oxidation (including rapid thermal techniques), wet anodization, vapour-phase technique (chemical vapour deposition), and plasma anodization or oxidation. [Campbell, 2001]

2.2 Silicon Dioxide

Of all advantages of silicon for the formation of semiconductor devices, the ease of growing of a silicon dioxide layer is perhaps the most useful. Whenever a silicon surface is exposed to oxygen, it is converted to silicon dioxide (Figure 2.1) [Campbell, 2001]. Silicon dioxide is composed of one

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