



UniMAP

A Novel Large-Bit-Size Architecture and
Microarchitecture for the Implementation of
Superscalar Pipeline VLIW Microprocessors

by

Lee, Weng Fook

0440210010

A thesis submitted

In fulfilment of the requirements for the degree of

Doctor of Philosophy

School of Computer & Communication Engineering

Universiti Malaysia Perlis

Year 2008

© Copyright by

Lee, Weng Fook

2008

© This item is protected by original copyright

Acknowledgement

I would like to take this opportunity to thank my advisor, Prof Dr Ali Yeon, for his valuable guidance throughout my years at Universiti Malaysia Perlis. His advice and help plays a major pivotal role in my accomplishing of the dissertation, not to mention his constant hard work in promoting my research.

I would also like to thank my dear friend Dr Bala Amawasai for his constant encouragement in pursuing my research work. To all the staff at Universiti Malaysia Perlis, of which have been generously helpful throughout my research, thank you for your great support. And to the directors of Emerald Systems Design Center, thank you for your generosity in financing my research work and allowing me to use the valuable compute resources on weekends.

A special word of thanks to Prof Dr Kasmiran Jumari, Prof Dr Nukala S. Murthy and Prof Dr Syed Alwee for their valuable feedback on this research, Prof Dr Mohd Zaki for chairing the viva voce session, Dr R. Badlishah for co-supervising the viva voce session and to Norzaililah Zainoddin for arranging the viva voce session.

Finally, a great thank you to my wife for being able to put up with me, especially during all those weekends that I had missed out with her to work on this dissertation.

Abstract

Microprocessors have grown tremendously in its computing and data crunching capability since the early days of the invention of a microprocessor. Today, most microprocessors in the market are at 32 bits, while the latest microprocessors from IBM, Intel and AMD are at 64 bits. To further grow the computational capability of a microprocessor, there are two possible paths. One method is to increase the bit size of the microprocessor to 128/256/512 bits. The larger the bitsize, the more data can be crunched at any one time. The second method is to implement multiple microprocessor core in a single microprocessor unit. For example, the Intel's Pentium 4 Dual Core and AMD's Athlon Dual Core both have two microprocessor core within a single microprocessor unit. Latest from Intel and AMD are quad core microprocessors with either a configuration of pseudo-quad core or full quad core within a single microprocessor unit. In a pseudo-quad core configuration, two silicon each consists dual core microprocessor is packaged within a single microprocessor unit while a full quad core consists of four microprocessor core on one silicon packaged within a single microprocessor unit.

Both methods have its advantages and disadvantages. Both methods yields different design issues and have different engineering limitations. This work explores the method of increasing the data bus size of the microprocessor from 32/64 bits to 128/256/512 bits to allow for more data crunching capability.

In the course of this work, a superscalar pipeline 64 bits VLIW microprocessor with 4 stages (fetch, decode, execute, writeback) and 3 parallel pipes is implemented on a TSMC 0.35 micron process. The implementation is then expanded to 128/256/512 bits using the same TSMC 0.35 micron process. To prove the concept that such a large bit size VLIW microprocessor can indeed be implemented, the said VLIW microprocessor

of bitsize 64/128/256 is programmed on an Altera Stratix 2 EP2S180F1508I4 FPGA and back annotated for verification.

In the TSMC 0.35 micron process implementation of the work, the critical path of the VLIW microprocessor of data bus size 128/256/512 is analyzed with its worst path within the adder of the ALU in the execute stage. Different adder architectures are investigated for suitability on synthesis implementation of large data bus size adder for efficient usage within the ALU. An adder algorithm using repetitive constructs in a parallel algorithm that allows for efficient and optimal synthesis for large data bus size is proposed as a suitable implementation for the adder within the ALU.

This work has two important findings. One is the proposed adder architecture synthesis of a large bit size adder that provides for improved performance-gatecount-product compared to conventional adder architecture synthesis. Second is the proof of concept that a large bit size VLIW microprocessor is possible by implementing a 64/128/256 bits data size on an Altera Stratix 2 EP2S180F1508I4 FPGA.

Abstrak

Mikropemproses telah berkembang dengan pesat dalam arena pemkomputeran dan pemprosesan data. Hari ini, kebanyakan mikropemproses di pasaran adalah bersaiz 32 bit, sementara mikropemproses yang terbaru dari IBM, Intel dan AMD adalah 64 bit. Terdapat dua kaedah yang boleh dilaksanakan bagi meningkatkan keupayaan sesuatu mikropemproses. Satu kaedahnya adalah dengan meningkatkan saiz bit mikropemproses kepada 128/256/512 bit. Lebih besar saiz bit, lebih banyak data yang boleh diproses dalam satu masa. Kaedah yang kedua adalah dengan melaksanakan pelbagai teras mikropemproses dalam satu unit mikropemproses. Sebagai contoh, Pentium 4 Dual Core dari Intel dan Athlon Dual Core dari AMD kedua-duanya mempunyai dua teras mikropemproses dalam satu unit mikropemproses. Yang terbaru dari Intel dan AMD adalah *quad core microprocessor* yang mempunyai dua konfigurasi, samada dengan konfigurasi *pseudo-quad core* atau *full quad core* dalam satu unit mikropemproses. Dalam konfigurasi *pseudo-quad core*, dua silicon yang mana setiap satu mengandungi dua teras mikropemproses disatukan dalam satu unit mikropemproses sementara *full quad core* mengandungi empat teras mikropemproses dalam satu silicon yang telah di satukan dalam satu unit mikropemproses.

Kedua-dua kaedah ini mempunyai kebaikan dan keburukannya sendiri. Kedua-dua kaedah menghasilkan rekaan yang berbeza dan mempunyai had limit kejuruteraan yang berbeza. Kajian ini menjelajah kaedah meningkatkan saiz *data bus* mikropemproses dari 32/64 bit kepada 128/256/512 bit untuk membenarkan lebih banyak kebolehan pemprosesan data.

Dalam hal ini *superscalar pipeline* 64 bits mikropemproses VLIW dengan 4 kategori (mengambil, menyahkod, melaksanakan, menulis balik) dan 3 sambungan selari dilaksanakan dengan menggunakan fabrikasi proses TSMC 0.35 mikron..

Perlaksanaan ini kemudian dikembangkan kepada 128/256/512 bit dengan menggunakan fabrikasi proses yang sama. Untuk membuktikan bahawa konsep saiz bit mikropemproses VLIW yang besar memang boleh dilaksanakan secara praktikal, mikropemproses VLIW dengan saiz bit 64/128/256 di programkan dalam Altera Stratix 2 EP2S180F150814 FPGA dan disimulasikan FPGA tersebut untuk pengesahan fungsi mikropemproses tersebut.

Dalam pelaksanaan kajian ini menggunakan fabrikasi proses TSMC 0.35 mikron, bahagian yang paling kritikal untuk mikropemproses VLIW dengan *data bus* bersaiz 128/256/512 adalah laluan penambah dalam ALU. Perbezaan senibina untuk jenis penambah yang berbeza di kaji untuk kesesuaian dalam pelaksanaan ALU yang mempunyai *data bus* yang bersaiz besar. Algoritma penambah menggunakan konstruk yang berulang yang menghasilkan sintesis litar digital yang optimal untuk saiz *data bus* yang besar dicadangkan sebagai implementasi yang sesuai untuk penambah dalam ALU.

Kajian ini mempunyai dua penemuan kejuruteraan yang penting. Penemuan pertama adalah cadangan algoritma penambah untuk saiz bit yang besar yang menyediakan peningkatan pencapaian prestasi-gatecount-produk berbanding dengan senibina penambahan yang konvensional. Penemuan kedua adalah pembuktian konsep yang mikropemproses VLIW dengan saiz bit yang besar memang boleh dilaksanakan secara praktikal dengan mengimplementasikan mikropemproses tersebut dengan saiz *data bus* 64/128/256 bit pada Altera Stratix 2 EP2S180F150814 FPGA.

Table Of Contents

1	INTRODUCTION.....	21
1.1	DATA CRUNCHING POWER OF MICROPROCESSORS	24
1.1.1	<i>Increasing Bit Size To Improve Data Crunching Power of Microprocessors</i>	26
1.1.2	<i>Multiple Microprocessor Core To Improve Data Crunching Power of Microprocessors</i>	28
1.2	MOTIVATION	30
1.3	RELATED RESEARCH WORK	31
1.4	OBJECTIVE/GOAL OF RESEARCH	33
1.5	INITIAL CONDITION – START OF RESEARCH	35
1.6	TYPES OF MICROPROCESSOR	37
1.7	TYPES OF MICROPROCESSOR ARCHITECTURE	39
1.7.1	<i>VLIW Microprocessor</i>	41
1.8	SUMMARY	45
2	DESIGN METHODOLOGY	46
2.1	TECHNICAL SPECIFICATION	47
2.1.1	<i>Instruction Set of VLIW Microprocessor</i>	50
2.1.2	<i>Definition of Opcode for VLIW Instruction Set</i>	52
2.1.3	<i>Definition of VLIW Instruction</i>	61
2.2	ARCHITECTURAL SPECIFICATION.....	63
2.3	MICRO-ARCHITECTURE SPECIFICATION.....	71
2.4	SUMMARY	85
3	RTL CODING, TESTBENCHING AND SIMULATION OF 64 BIT VLIW MICROPROCESSOR.....	86
3.1	MODULE <i>FETCH</i> RTL CODE	93
3.2	MODULE <i>DECODE</i> RTL CODE	98
3.3	MODULE <i>REGISTER FILE</i> RTL CODE	101
3.4	MODULE <i>EXECUTE</i> RTL CODE	111

3.5	MODULE <i>WRITEBACK</i> RTL CODE.....	121
3.6	MODULE <i>VLIWTOP</i> RTL CODE.....	127
3.7	TESTBENCHES AND SIMULATION	128
3.7.1	<i>Creating and Using A Testplan</i>	129
3.8	SYNTHESIS.....	131
3.8.1	<i>Standard Cell Library</i>	132
3.8.2	<i>Design Constraints</i>	135
3.9	FORMAL VERIFICATION	136
3.10	PRE-LAYOUT STATIC TIMING ANALYSIS	137
3.11	LAYOUT.....	140
3.11.1	<i>Manual/Custom Layout</i>	142
3.11.2	<i>Semi Custom/Auto Layout</i>	143
3.11.3	<i>Auto Place And Route</i>	144
3.12	DRC / LVS.....	146
3.13	RC EXTRACTION	148
3.14	POST LAYOUT LOGIC VERIFICATION	149
3.15	POST LAYOUT PERFORMANCE VERIFICATION	150
3.16	TAPEOUT	151
3.17	LINKING FRONTEND AND BACKEND	152
3.18	POWER CONSUMPTION.....	157
3.19	ASIC DESIGN TESTABILITY	159
3.20	SUMMARY	162
4	IMPLEMENTATION OF LARGE BIT SIZE VLIW MICROPROCESSOR ON ASIC.....	164
4.1	DIFFERENT TYPES OF ADDER ARCHITECTURE.....	167
4.1.1	<i>Carry Save adder</i>	168
4.1.2	<i>Ripple Adder</i>	170
4.1.3	<i>Conditional Sum Adder</i>	171
4.1.4	<i>Carry select adder</i>	173
4.1.5	<i>Carry look ahead adder</i>	176
4.1.6	<i>Brent Kung adder</i>	179

4.1.7	<i>Sklansky adder</i>	180
4.1.8	<i>Kogge Stone adder</i>	181
4.1.9	<i>Han Carlson adder</i>	182
4.1.10	<i>Carry skip adder</i>	183
4.2	IMPLEMENTING HIGH SPEED AND COST EFFICIENT LARGE BIT SIZE ADDER	184
4.3	IMPLEMENTATION OF SYNTHESIS OF LARGE BIT SIZE ADDER USING CONVENTIONAL ADDER ARCHITECTURE.....	186
4.4	ARCHITECTURAL SYNTHESIS OF PARALLEL EXECUTION OF LARGE BIT SIZE ADDITION	190
4.5	SUMMARY	200
5	IMPLEMENTATION OF LARGE BIT SIZE VLIW MICROPROCESSOR ON FPGA	202
5.1	FPGA VERSUS ASIC.....	203
5.2	FPGA DESIGN METHODOLOGY	205
5.3	ANALYSIS OF FPGA IMPLEMENTATION RESULTS ON LARGE BIT SIZE VLIW MICROPROCESSOR	207
5.4	VERIFICATION OF VLIW MICROPROCESSOR ON FPGA	211
5.5	STRUCTURED ASIC.....	213
5.6	SUMMARY.....	215
6	DISCUSSION, CONCLUSION & FUTURE WORK	217
6.1	DISCUSSION & CONCLUSION.....	217
6.2	FUTURE WORK.....	222
	REFERENCES.....	223
	LIST OF PUBLICATIONS	235
	APPENDIX A TESTBENCHES AND SIMULATION RESULTS FOR VERIFYING THE 64 BIT VLIW MICROPROCESSOR.....	236
	APPENDIX B GATE LEVEL NETLIST OF THE 64 BIT VLIW MICROPROCESSOR	262
	APPENDIX C LAYOUT AND ATPG COVERAGE OF VLIW MICROPROCESSOR.....	268

**APPENDIX D TESTBENCHES AND SIMULATION RESULTS FOR VERIFYING
IMPLEMENTED VLIW MICROPROCESSOR ON FPGA275**

© This item is protected by original copyright

Table Of Figures

FIGURE 1	DIAGRAM SHOWING MICROPROCESSOR AS CORE OF MICRO-CONTROLLER	22
FIGURE 2	DIAGRAM SHOWING GROWTH OF MICROPROCESSOR.....	25
FIGURE 3	DIAGRAM SHOWING DUAL CORE MICROPROCESSOR.....	29
FIGURE 4	DIAGRAM SHOWING INSTRUCTION EXECUTION FOR PIPELINE MICROPROCESSOR.....	40
FIGURE 5	DIAGRAM SHOWING INSTRUCTION EXECUTION FOR SUPERSCALAR PIPELINE MICROPROCESSOR	40
FIGURE 6	DIAGRAM SHOWING INSTRUCTION EXECUTION FOR VLIW MICROPROCESSOR	41
FIGURE 7	DIAGRAM SHOWING DESIGN METHODOLOGY FLOW.....	46
FIGURE 8	DIAGRAM SHOWING A GENERIC ARCHITECTURE FOR VLIW MICROPROCESSOR.....	63
FIGURE 9	DIAGRAM SHOWING TOP LEVEL ARCHITECTURE.....	65
FIGURE 10	DIAGRAM SHOWING INTERFACE SIGNALS FOR VLIW MICROPROCESSOR	69
FIGURE 11	DIAGRAM SHOWING INTERFACE BETWEEN VLIW MICROPROCESSOR AND EXTERNAL SYSTEMS	70
FIGURE 12	DIAGRAM SHOWING MICRO-ARCHITECTURE OF MICROPROCESSOR	75
FIGURE 13	DIAGRAM SHOWING END OF TIMING PATH AT FLIP-FLOP	87
FIGURE 14	DIAGRAM SHOWING A DESIGN WITH POOR PARTITIONING.....	91
FIGURE 15	DIAGRAM SHOWING A DESIGN WITH GOOD PARTITIONING.....	91
FIGURE 16	DIAGRAM SHOWING INFINITE TIMING LOOP OF COMBINATIONAL LOGIC	92
FIGURE 17	DIAGRAM SHOWING INTERFACE SIGNALS FOR <i>FETCH</i> MODULE.....	96
FIGURE 18	DIAGRAM SHOWING INTERFACE SIGNALS FOR <i>DECODE</i> MODULE.....	100
FIGURE 19	DIAGRAM SHOWING INTERFACE SIGNALS FOR <i>REGISTER FILE</i> MODULE.....	106
FIGURE 20	DIAGRAM SHOWING TWO VLIW INSTRUCTIONS PASSING THROUGH THE VLIW MICROPROCESSOR 4 STAGE PIPELINE	108
FIGURE 21	DIAGRAM SHOWING TWO VLIW INSTRUCTIONS PASSING THROUGH THE VLIW MICROPROCESSOR 4 STAGE PIPELINE WITH REGISTER BYPASSING	109
FIGURE 22	DIAGRAM SHOWING INTERFACE SIGNALS FOR <i>EXECUTE</i> MODULE.....	117
FIGURE 23	DIAGRAM SHOWING INTERFACE SIGNALS FOR <i>WRITEBACK</i> MODULE	126
FIGURE 24	DIAGRAM SHOWING INTERFACE SIGNALS FOR <i>VLIWTOP</i> MODULE	127

FIGURE 25	DIAGRAM SHOWING A SETUP TIME VIOLATION	137
FIGURE 26	DIAGRAM SHOWING TIMING OF <i>NETB</i> WITH A SETUP TIME REQUIREMENT	138
FIGURE 27	DIAGRAM SHOWING A HOLD TIME VIOLATION	139
FIGURE 28	DIAGRAM SHOWING PHYSICAL LAYOUT OF AN INVERTER	140
FIGURE 29	DIAGRAM SHOWING DESIGN FLOW FOR POST LAYOUT LOGIC VERIFICATION	149
FIGURE 30	DIAGRAM SHOWING DESIGN FLOW FOR POST LAYOUT PERFORMANCE VERIFICATION ...	150
FIGURE 31	DIAGRAM SHOWING CLOCK ROUTING FOR DIFFERENT FLIP-FLOPS	154
FIGURE 32	DIAGRAM SHOWING CLOCK SKEW OF DIFFERENT FLIP-FLOPS	155
FIGURE 33	DIAGRAM SHOWING AN AND GATE FOR GATED CLOCK	157
FIGURE 34	DIAGRAM SHOWING A REGISTER REPLACED BY SCAN REGISTER	160
FIGURE 35	DIAGRAM SHOWING A BOUNDARY SCAN CHAIN WITH JTAG STATE CONTROLLER	161
FIGURE 36	DIAGRAM SHOWING CRITICAL PATH DELAY GOING THROUGH THE 64 BIT ADDER IN EXECUTE MODULE	165
FIGURE 37	DIAGRAM SHOWING CSA REDUCING THREE OPERANDS INTO TWO OPERANDS	168
FIGURE 38	DIAGRAM SHOWING WALLACE TREE CSA	168
FIGURE 39	DIAGRAM SHOWING RIPPLE ADDER	170
FIGURE 40	DIAGRAM SHOWING CONDITIONAL SUM ADDER FOR 2 BITS ADDITION	171
FIGURE 41	DIAGRAM SHOWING CONDITIONAL SUM ADDER FOR 4 BITS ADDITION	172
FIGURE 42	DIAGRAM SHOWING CARRY SELECT ADDER FOR 16 BITS ADDITION	175
FIGURE 43	DIAGRAM SHOWING COMBINATIONAL BLOCK FOR CARRY LOOK AHEAD ADDER	177
FIGURE 44	DIAGRAM SHOWING GENERATION OF $S[n]$ AND COUT OF CARRY LOOK AHEAD ADDER .	178
FIGURE 45	DIAGRAM SHOWING PARALLEL PREFIX TREE FOR BRENT KUNG ADDER	179
FIGURE 46	DIAGRAM SHOWING PARALLEL PREFIX TREE FOR SKLANSKY ADDER	180
FIGURE 47	DIAGRAM SHOWING PARALLEL PREFIX TREE FOR KOGGE STONE ADDER	181
FIGURE 48	DIAGRAM SHOWING PARALLEL PREFIX TREE FOR HAN CARLSON ADDER	182
FIGURE 49	DIAGRAM SHOWING CARRY SKIP ADDER	183
FIGURE 50	DIAGRAM SHOWING DELAY OF ADDER ARCHITECTURE IMPLEMENTED ON TSMC 0.35 MICRON PROCESS TECHNOLOGY	187
FIGURE 51	DIAGRAM SHOWING GATE COUNT OF ADDER ARCHITECTURE IMPLEMENTED ON TSMC 0.35 MICRON PROCESS TECHNOLOGY	188

FIGURE 52	HIGH LEVEL DESCRIPTION OF ALGORITHM FOR ARCHITECTURAL SYNTHESIS OF LARGE BIT SIZE ADDER	191
FIGURE 53	ALGORITHM FOR ADDITION OF TWO 64 BIT HEXADECIMAL NUMBERS	192
FIGURE 54	SYNTHESIZED CIRCUIT OF 2^N BIT ADDER.....	193
FIGURE 55	PLOTTED GRAPH OF DELAY-AREA PRODUCT OF DIFFERENT ADDER ARCHITECTURE ON DIFFERENT BITSIZE.....	199
FIGURE 56	DIAGRAM SHOWING FPGA DESIGN METHODOLOGY.....	205
FIGURE 57	NORMALIZED POWER (MW) – DELAY (NS) PRODUCT ON DIFFERENT DATA BUS SIZE.....	208
FIGURE 58	FPGA CELL ELEMENT USAGE FOR TEST VEHICLE ON DIFFERENT DATA BUS SIZE	209
FIGURE 59	DIAGRAM SHOWING FLOW FOR VERIFYING FPGA IMPLEMENTATION.....	212
FIGURE 60	DIAGRAM SHOWING FLOW FOR CONVERSION TO STRUCTURED ASIC	214
FIGURE 61	DIAGRAM SHOWING SIMULATION RESULT OF TESTBENCH 1 FOR BARREL SHIFT LEFT, SUBTRACT AND MULTIPLY.....	243
FIGURE 62	DIAGRAM SHOWING READ SIMULATION RESULT FOR TESTBENCH 1.....	244
FIGURE 63	DIAGRAM SHOWING REGISTER BYPASS CONDITIONS OF TESTBENCH 2.....	252
FIGURE 64	DIAGRAM SHOWING JUMP AND FLUSH CONDITION FOR TESTBENCH 3	260
FIGURE 65	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (80NS – 120NS).....	300
FIGURE 66	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (120NS – 160NS).....	301
FIGURE 67	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (160NS – 200NS).....	302
FIGURE 68	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (200NS – 240NS).....	303
FIGURE 69	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (240NS – 280NS).....	304
FIGURE 70	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (280NS – 320NS).....	305
FIGURE 71	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (320NS – 360NS).....	306

FIGURE 72	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (360NS – 400NS)	307
FIGURE 73	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (400NS – 440NS)	308
FIGURE 74	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (440NS – 480NS)	309
FIGURE 75	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (80NS – 120NS)	335
FIGURE 76	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (120NS – 160NS)	336
FIGURE 77	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (160NS – 200NS)	337
FIGURE 78	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (200NS – 240NS)	338
FIGURE 79	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (240NS – 280NS)	339
FIGURE 80	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (280NS – 320NS)	340
FIGURE 81	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (320NS – 360NS)	341
FIGURE 82	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (360NS – 400NS)	342
FIGURE 83	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (400NS – 440NS)	343
FIGURE 84	DIAGRAM SHOWING SIMULATION RESULT OF IMPLEMENTATION OF VLIW MICROPROCESSOR ON FPGA (440NS – 480NS)	344

Table Of Examples

TESTBENCH 1: TESTBENCH VERIFYING BARREL SHIFT LEFT, SUBTRACT, MULTIPLY AND READ	236
TESTBENCH 2: TESTBENCH VERIFYING MULTIPLE REGISTER BYPASS CONDITION BETWEEN • OPERATION1, OPERATION2 AND OPERATION3	245
TESTBENCH 3: TESTBENCH VERIFYING A <i>FLUSH</i> AND <i>JUMP</i> CONDITION DURING COMPARE OPERATION	253
TESTBENCH 4: TESTBENCH VERIFYING VLIW MICROPROCESSOR ON FPGA (ADD, SUB, MUL, LOAD, READ, XOR, NAND)	275
TESTBENCH 5: TESTBENCH VERIFYING VLIW MICROPROCESSOR ON FPGA (NOR, NOT, SHIFT RIGHT, SHIFT LEFT, BARREL SHIFT RIGHT, BARREL SHIFT LEFT)	310

© This item is protected by original copyright

List Of Tables

TABLE 1.	REGISTER ADDRESS FOR INTERNAL REGISTER OF <i>REGISTER FILE</i>	48
TABLE 2.	TABLE SHOWING THE OPERATION CODE FOR THE VLIW MICROPROCESSOR INSTRUCTION	
SET	50
TABLE 3.	TABLE SHOWING COMBINATION OF OPERATION CODE AND INTERNAL REGISTER	
ADDRESSES TO FORM AN OPERATION	51
TABLE 4.	BIT FORMAT FOR OPERATION CODE “NOP”	52
TABLE 5.	BIT FORMAT FOR OPERATION CODE <i>ADD</i>	53
TABLE 6.	BIT FORMAT FOR OPERATION CODE <i>SUB</i>	53
TABLE 7.	BIT FORMAT FOR OPERATION CODE <i>MUL</i>	54
TABLE 8.	BIT FORMAT FOR OPERATION CODE <i>LOAD</i>	54
TABLE 9.	BIT FORMAT FOR OPERATION CODE <i>MOVE</i>	55
TABLE 10.	BIT FORMAT FOR OPERATION CODE <i>READ</i>	55
TABLE 11.	BIT FORMAT FOR OPERATION CODE <i>COMPARE</i>	56
TABLE 12.	BIT FORMAT FOR OPERATION CODE <i>XOR</i>	56
TABLE 13.	BIT FORMAT FOR OPERATION CODE <i>NAND</i>	57
TABLE 14.	BIT FORMAT FOR OPERATION CODE <i>NOR</i>	57
TABLE 15.	BIT FORMAT FOR OPERATION CODE <i>NOT</i>	57
TABLE 16.	BIT FORMAT FOR OPERATION CODE <i>SHIFT LEFT</i>	58
TABLE 17.	BIT FORMAT FOR OPERATION CODE <i>SHIFT RIGHT</i>	59
TABLE 18.	BIT FORMAT FOR OPERATION CODE <i>BARREL SHIFT LEFT</i>	59
TABLE 19.	BIT FORMAT FOR OPERATION CODE <i>BARREL SHIFT RIGHT</i>	60
TABLE 20.	DESCRIPTION OF VLIW MICROPROCESSOR INTERFACE SIGNALS	66
TABLE 21.	DESCRIPTION OF INTER-MODULE SIGNALS FOR MICRO-ARCHITECTURE OF VLIW	
MICROPROCESSOR	76
TABLE 22.	TABLE SHOWING INTERFACE SIGNALS OF <i>FETCH</i> MODULE.....	93
TABLE 23.	TABLE SHOWING INTERFACE SIGNALS OF <i>DECODE</i> MODULE.....	98
TABLE 24.	TABLE SHOWING INTERFACE SIGNALS OF <i>REGISTER FILE</i> MODULE	101
TABLE 25.	TABLE SHOWING INTERFACE SIGNALS OF <i>EXECUTE</i> MODULE.....	111

TABLE 26.	TABLE SHOWING INSTRUCTION EXECUTION THROUGH THE PIPE STAGES	118
TABLE 27.	TABLE SHOWING INTERFACE SIGNALS OF <i>WRITEBACK</i> MODULE	121
TABLE 28.	TABLE SHOWING AN EXAMPLE OF A SIMPLE TESTPLAN FOR THE VLIW MICROPROCESSOR	129
TABLE 29.	TABLE SHOWING CRITICAL PATH DELAY THROUGH 64/128/256/512 BIT VLIW MICROPROCESSOR (NS).....	164
TABLE 30.	TABLE SHOWING DELAY OF DIFFERENT ADDER ARCHITECTURE IMPLEMENTED ON TSMC 0.35 MICRON PROCESS TECHNOLOGY (NS)	186
TABLE 31.	TABLE SHOWING GATE COUNT OF DIFFERENT ADDER ARCHITECTURE IMPLEMENTED ON TSMC 0.35 MICRON PROCESS TECHNOLOGY	186
TABLE 32.	CRITICAL PATH DELAY FOR DIFFERENT BIT SIZE FOR TD_1 AND TD_2	195
TABLE 33.	DELAY AND GATE COUNT OF IMPLEMENTATION OF PROPOSED ALGORITHM ON TSMC 0.35 MICRON	196
TABLE 34.	NORMALIZED DELAY (NS) - AREA (GATECOUNT) PRODUCT FOR DIFFERENT ADDER ARCHITECTURE AND DIFFERENT BITSIZE	197
TABLE 35.	TABLE DESCRIBING ADVANTAGES AND DISADVANTAGES OF FPGA AND ASIC [3, 4, 54, 83, 88, 89]	203
TABLE 36.	TABLE SHOWING NORMALIZED POWER (MW) - DELAY (NS) PRODUCT OF DIFFERENT BIT SIZE IMPLEMENTATION ON ALTERA STRATIX 2 EP2S180F1508I4 FPGA.	208
TABLE 37.	TABLE SHOWING FPGA ELEMENT USAGE OF DIFFERENT BIT SIZE IMPLEMENTATION ON ALTERA STRATIX 2 EP2S180F1508I4 FPGA.	208

List of Abbreviations

ADK	ASIC Design Kit
ALU	Arithmetic Logic Unit
ALUT	Altera Look Up Table
AMD	Advanced Micro Devices
APR	Auto Place and Route
ASIC	Application Specific Integrated Circuit
ATM	Auto Teller Machine
ATPG	Automatic Test Pattern Generation
BIST	Built In Self Test
CISC	Complex Instruction Set Computing
CPU	Central Processing Unit
CSA	Carry Save Adder
DRC	Design Rule Check
Dspf	Detailed Standards Parasitic Format
EPROM	Erasable Programmable Read-Only Memory
FA	Full Adder
FPGA	Field Programmable Gate Array
GDSII	Graphic Data System II
IBM	International Business Machine
IC	Integrated Circuit
ILP	Instruction Level Parallelism
IO	Input Output
JTAG	Joint Test Action Group

LVS	Layout Versus Schematic
OS	Operating System
PDA	Personal Digital Assistant
POS	Point of Sale
RAM	Random Access Memory
RC	Resistance Capacitance
RISC	Reduced Instruction Set Computing
ROM	Read Only Memory
RTL	Register Transfer Level
SDL	Schematic Driven Layout
Sdf	Standard Delay Format
Spf	Standard Parasitic Exchange Format
TSMC	Taiwan Semiconductor Manufacturing Company
VLIW	Very Long Instruction Word

© This item is protected by original copyright

1 Introduction

Micro-processors and micro-controllers are widely used in the world today. It is used in everyday electronic systems, be it a system used in the industries or a system used by consumers. Complex electronic systems such as ATM machine, POS systems, financial systems, transaction systems, control systems, database systems all uses some form of micro-controller or micro-processor as the core of their system. Consumer electronic systems such as home security systems, credit cards, microwave ovens, cars, cellphones, PDA, refrigerators and other daily appliances have within the core of the system either a micro-controller or micro-processor.

What is a micro-controllers and micro-processor? If they are such a big part of our daily life, what exactly are their function?

Micro-processors and micro-controllers are very similar in nature. In fact, from a top level perspective, a micro-processor is the core of a micro-controller. A micro-controller basically consists of a micro-processor as its CPU (central processing unit) with peripheral logic surrounding the micro-processor core. As such it can be viewed that a micro-processor is the building block for a micro-controller (Refer Figure 1).

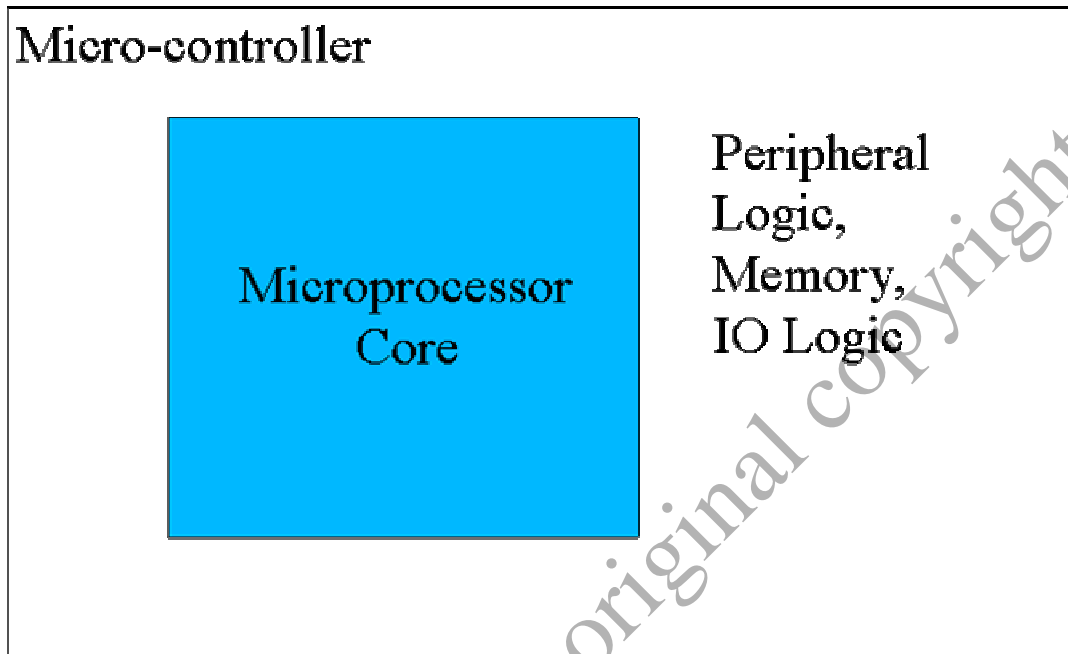


Figure 1. Diagram Showing Microprocessor as Core of Micro-controller

A more general view of a micro-controller is that it is a multi purpose IC chip that has circuitry elements that enables it to perform certain tasks required of an electronic system. A micro-controller is a single IC chip solution that can be used to perform dedicated tasks within a system, such as controlling a pump, controlling a car's engine electronic system, heart of a home security system and many others. A micro-controller consists of:

1. non volatile memory such as EPROM (Electronic Programmable Read Only Memory), ROM (Read Only Memory) that is used to store the systems' central program which allows the system to perform a specific task
2. volatile memory such as RAM (Random Access Memory) that can be used by the micro-controller for storage of information
3. peripheral logic that allows the system to have direct access to IO (input/output)

A microprocessor forms the CPU (central processing unit) of the microcontroller. Within the microprocessor is circuitry that enables the microprocessor to do arithmetic functions, logic functions and execution of instructions provided to the microprocessor.

Our daily lives are filled with usage of a computer, whether we are aware of it or not. For example, when we go to a bank and make a withdrawal using an ATM machine, the ATM machine would identify us and our bank account using an ATM card issued by the bank. That information is relayed from the ATM machine to a central computer system that transmit information back to the ATM machine on the amount of savings in the account and how much can be withdrawn at that moment. When we do decide to withdraw a certain sum of money, that transaction is automatically recorded in the bank's central computer system and the corresponding bank account. This process is automated within a computer system, and at the very heart of the computer systems lies many microprocessors.

Computers that we use daily at home or at work have a microprocessor as its brain. The microprocessor does all the necessary functions of the computer when we are using a word editor, or a spreadsheet or even preparing our electronic presentation.

Computers cannot function without a microprocessor.

1.1 Data Crunching Power Of Microprocessors

A microprocessor's capability to crunch data is dependent on its bus width. The larger the bus width the more data that it can crunch at any one time. For example, the crunching capability of a 32 bit microprocessor is at a comparable doubling factor of a 16 bit microprocessor. Therefore having a microprocessor with larger bus size allows for more data crunching capability. However there is a drawback to using larger bus size. The larger the bus size, the greater amount of logic is required, and the larger the die size. Most microprocessors in the market today such as Intel's Xeon and EMT64 microprocessor, AMD's Athlon 64 and Opteron microprocessor, IBM's PowerPC microprocessor are 64 bit microprocessors. They are able to crunch data at 64 bits at a time.

Moving forward, in order to have a microprocessor to have more data crunching capability, there is two methods of progress:

1. increase the bit size from 64 bits to 128/256/512 bits and beyond
2. increase the amount of microprocessor core in a single microprocessor

Method (1) increases the bus width to accommodate for more data crunching capability, while method (2) uses multiple microprocessor core in a single microprocessor to allow for multiple activities. Each method have its advantages and disadvantages.

Figure 2 shows the two methods used for growing the computation capability of the microprocessor.