CHAPTER 2

LITERATURE REVIEW

2.1 The main purpose of isolation technique

The need for a reduction of the spacing between devices in integrated circuits has led to the development of several device isolation process schemes. In this chapter, there is an overview of the most important trends in isolation technologies, starting with the conventional LOCOS structure. A novel isolation structure that combines several of the features used in advanced isolation structures is demonstrated and is used to investigate the trade-offs between the process steps that lead to a reduction in active area loss and the electrical performance of the isolation structure in terms of junction leakage. Before the invention of the planar technology, transistors and diodes were usually fabricated as mesa structures. Surface leakage currents were a big problem in these devices.

However the discovery by Atalla et al. that a thermally grown oxide on silicon could dramatically reduce the leakage current by passivating the surface, led directly to the development of the first fundamental oxide isolation structure for integrated circuits, the planox process. A breakthrough in the field of isolation technology came in 1970 when Appels et al. realized that Si3N4 was resistant to oxidation. They applied this concept to selectively oxidize silicon and develop the 'Local Oxidation of Silicon', or LOCOS, process to electrically isolate devices.

2.2 Conventional Local Oxidation (LOCOS)

2.2.1 Semi-recessed Local Oxidation

Semi-recessed LOCOS is the early technique for isolation process before another technique has been invented. Semi-recessed LOCOS is fewer complexes for isolation process compared with the fully-recessed LOCOS and results in less process induces defects in the silicon substrate. The process to form the fully-recessed locos comprising several steps. Pad oxide should be at least 1/3 nitride thickness to work as a stress relief layer. Nitride thickness needs to be thick enough to not be consumed during field oxide growth. Etching off nitride and pad oxide after field oxide is often done wet. Top of nitride is oxidized so it needs an HF etch followed by Hot (200^0 C) Phosphoric Acid etch or plasma etch. Kooi oxide growth is a sacrificial oxide to clean up any silicon nitride formed under the pad oxide by diffusion of NH_3 (from water nitride reaction) through pad oxide [1]. The cross-section of the semi-recessed locos is shown in Figure 2.0:

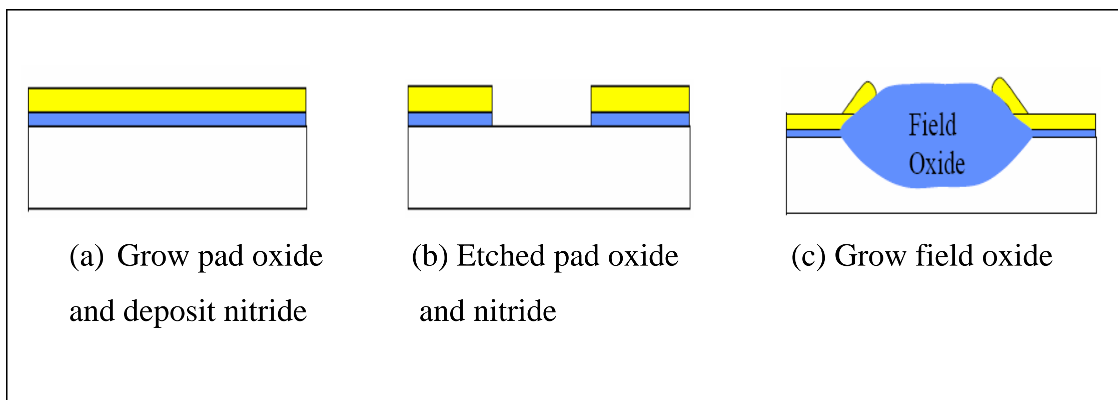


Figure 2.0: Cross section for semi-recessed LOCOS [1]

2.2.2 Fully-recessed local oxidation (LOCOS)

Several conventional, fully recessed oxide LOCOS methods have been developed for bipolar integrated-circuit application. Such fully oxide-isolation processes allow higher performance bipolar ICs to be fabricated than if junction isolation is used. The collar of SiO_2 that forms the sidewall isolation eliminates the sidewall contribution to collector-to-substrate and base-to-collector capacitances, thereby increasing the cutoff frequency of oxide-isolated transistor to 3-5 GHz- well above the 1-GHz limit of junction-isolated devices [2].

In all these approaches, the basic semi-recessed LOCOS process is still followed, with the following modification: After the nitride and pad oxide have been defined, the silicon epitaxy, pad oxide layer and nitride layer are etched as illustrated in Figure 4 (c). These steps can be done using anisotropic wet etching or isotropic etching. Next the field oxide is growth downward and extends completely through the epitaxy layer as shown in Figure 2.1 (d) [2].

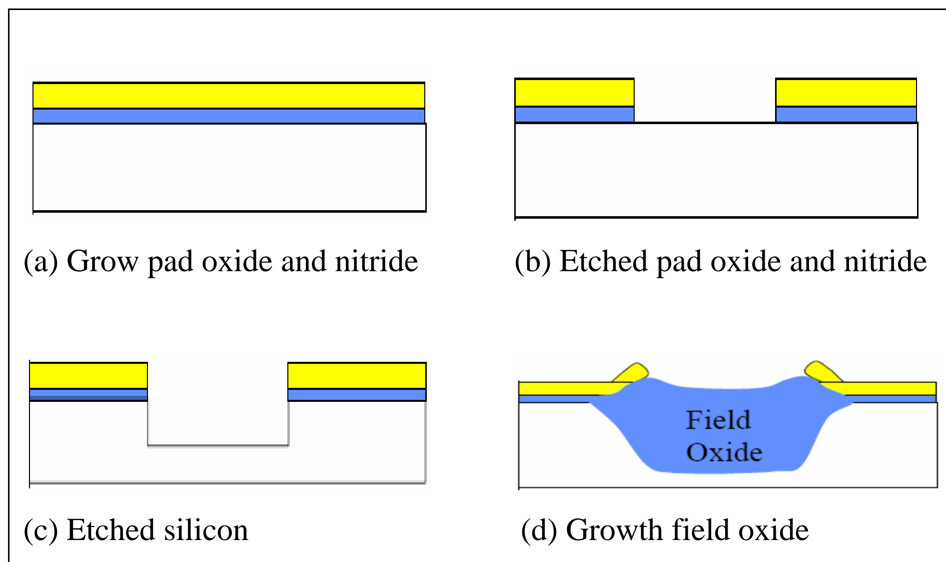


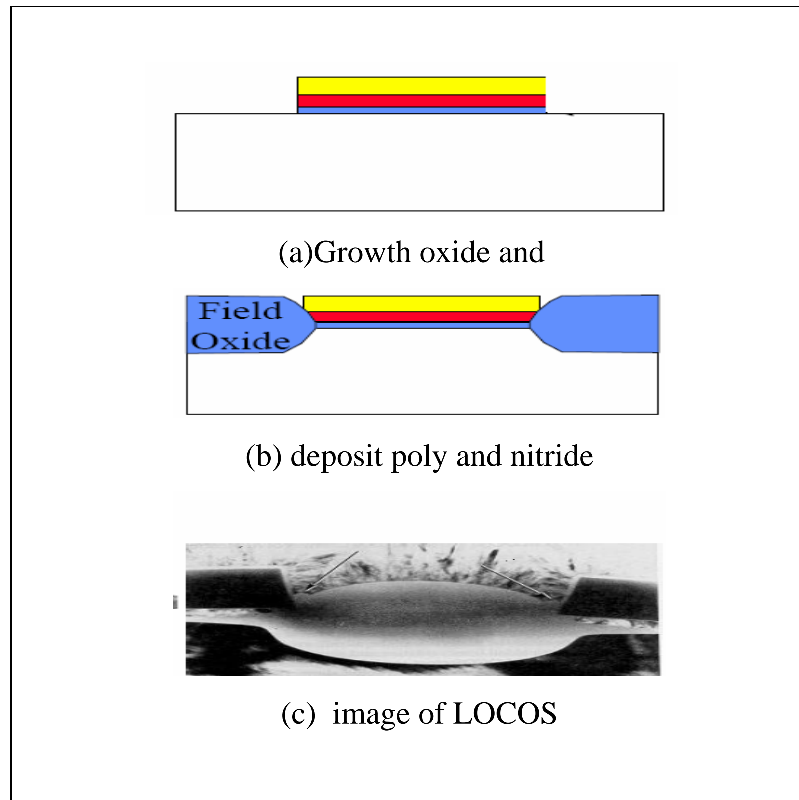
Figure 2.1: Cross section for fully-recessed LOCOS [2].

2.3 Advanced semi-recessed LOCOS

2.3.1 Poly-buffered LOCOS

Poly buffered LOCOS (PBL) has emerged as the most likely advanced isolation technique to achieve the benefits of LOCOS without suffering excessive process complexity. PBL incorporates the use of a stress-relief polysilicon layer between the pad oxide and nitride. The polysilicon buffer layer allows thinning of the pad oxide and/or thickening of the nitride, both of which reduce the bird's beak. Unfortunately, PBL suffers from two potentially significant drawbacks [3].

First, PBL field oxide exhibits less recess into the silicon substrate which increases topography and decreases the effective electrical source-to-drain separation. Second, the PBL oxidation mask stack is often difficult to photolithographically define and etch while maintaining tight critical dimension control. The sequences process to form poly-buffered LOCOS is simplified in Figure 5 above. Firstly, the pad oxide layer is grown using dry oxidation and thickness of pad oxide is about 200 Å to 600 Å. Then, the second layer of polysilicon is deposit using plasma enhanced chemical vapor deposition (PECVD) with the thickness of polysilicon range about 500 Å to 600 Å. The poly layer is used as a stress relief layer. Then nitride layer is deposit using PECVD. After the pattern transfer the layer of nitride, poly will be etching to form an active area and continue with grow field oxide using wet oxidation. The image topography is shown above in Figure 2.2 (c) [3].



(a)Growth oxide and

(b) deposit poly and nitride

(c) image of LOCOS

Figure 2.2: Cross section for Poly-buffered LOCOS [3]

2.3.2 Sealed interface local oxidation (Silo)

In Sealed-Interface Local Oxidation (SILO) processing, a silicon nitride film is in intimate contact with the silicon surface. The ubiquitous native oxide is effectively eliminated by using nitrogen ion implantation into silicon or plasma-enhanced nitridation to form a 'sealing film' of about 100 Å thicknesses. The oxidation rate in both types of films is characterized and found to be nearly equivalent. A 100- Å film can mask the growth of 7000 Å of oxide at 950^0 C in wet oxygen. It is found that, with a sealed interface, the usual 'bird's beak' formation is completely suppressed in local oxidation [4].

An approximate theoretical analysis shows that even a very thin interfacial oxide, acting as a lateral diffusion path for the oxidant species, can lead to an appreciable bird's beak. With a sealed interface using a 90 Å film, the thick-oxide to bare-silicon transition region is found to be chisel-shaped, with approximately 45-deg slopes. The transition region is even more pronounced if a conventional LPCVD nitride film is deposited on the sealing film before patterning [4].

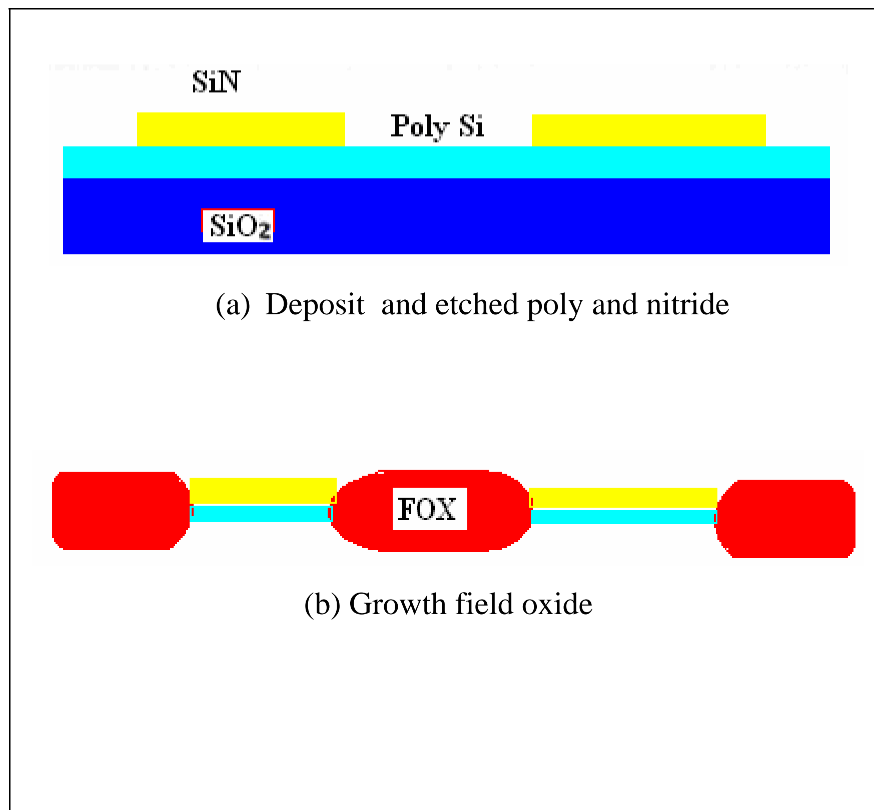


Figure 2.3: Cross section for sealed interface local oxidation [4].

2.4 Advanced fully-recessed LOCOS

2.4.1 Sidewall-masked isolation

The sidewall-masked isolation (SWAMI) technique has received much attention since it was introduced as a bird's-beak-free isolation scheme by Chiu et al. in 1982. Its main advantages over conventional LOCOS are an increase in packing density(due to limited lateral encroachment), no severe restrictions on the field-oxide thickness, improvement of the surface planarity, and complete elimination of the gate-oxide-thinning phenomenon (Kooi effect) [5].

SWAMI pad-oxide and CVD-nitride layers are formed and etched in the same manner as in conventional LOCOS. Grooves are then etched in the silicon to a depth of approximately half the desired field-oxide thickness. This is most often carried out by means of an orientation-dependent silicon etch, such as KOH. This produces recesses having sidewalls that are inclined about 60 when formed on a <100> surface. During field oxidation these sloping sidewalls help to reduce the stresses that contribute to the generation of edge defects [5].

A second stress-relief oxide layer is then grown, followed by the deposition of a second CVD nitride (which provides conformal coverage of the entire surface, including the sidewalls of the silicon recesses) where shown in Figure 3.4(a). This composite CVD SiO_2 layer is anisotropically etched in that field region so that it remains only on walls of the recessed silicon. Because the CVD oxide forms a spacer that protects part of the second nitride layer, this nitride forms a structure with a foot that extends partway into the exposed silicon at the bottom of the recess. After oxide spacer has been etched away, the final structure is a silicon mesa whose sidewalls are surrounded by the second nitride and oxide. At this point the channel-stop implant is performed, and the field oxide is grown.

In the latter step, the thin sidewall nitride is bent upward due to the expansion of the converted SiO2. The length of the foot of the nitride on the floor of the recessed silicon is selected to minimize the growth of the bird's beak into the active area. Finally the masking nitride/oxide layers are removed as shown in Figure 2.4(e) [5].

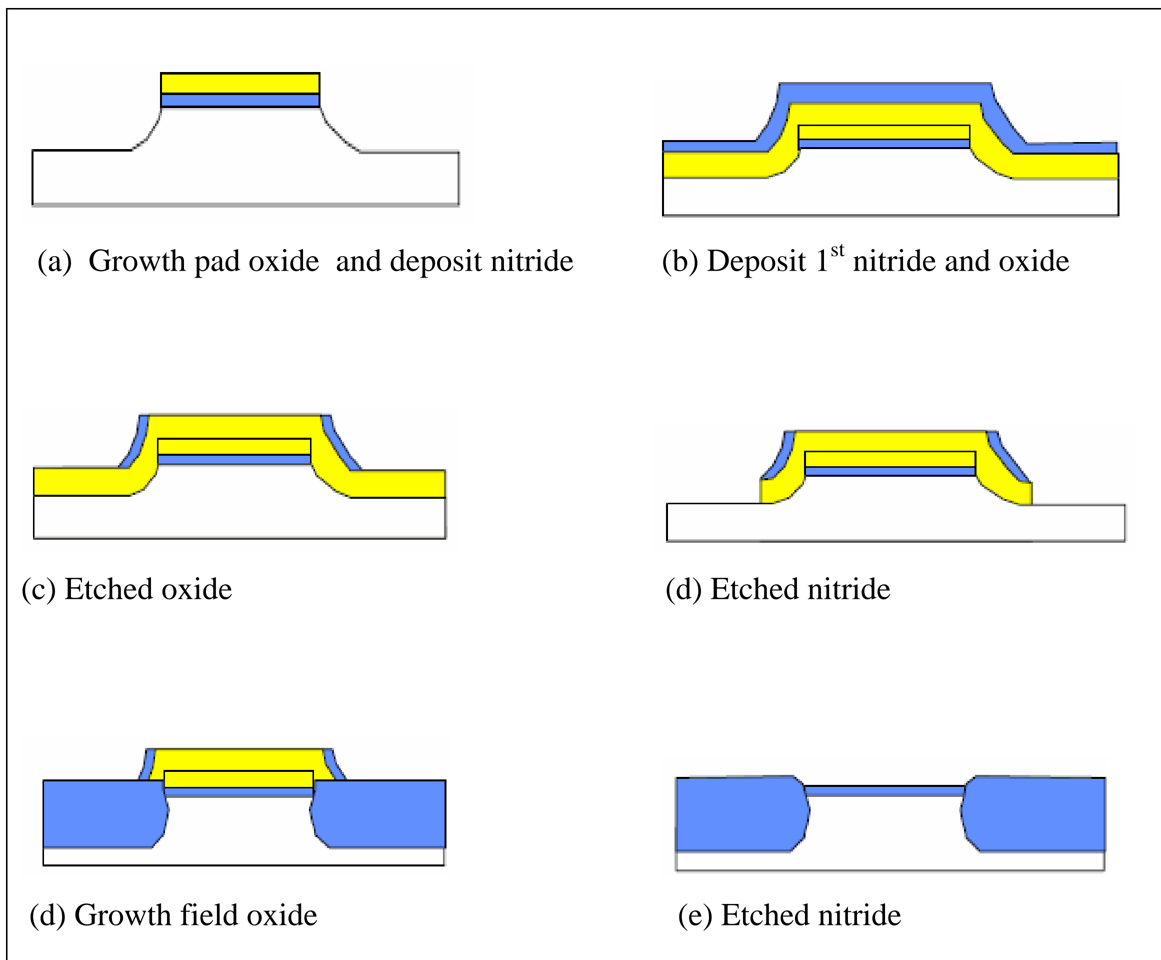


Figure 2.4: Cross section for Sidewall-masked isolation (SWAMI) [5].

2.4.2 Self-aligned planar-oxidation technology (SPOT)

Another modified SWAMI-like fully recessed LOCOS process that eliminates the bird's head and produces a highly planar surface with no observed dislocation generation has been reported. In this isolation process, called self-aligned planar-oxidation technology (SPOT), a conventional semi-recessed field oxide is first grown using high-pressure oxidation. This field oxide is then removed with a buffered HF using high-pressure oxidation. This field oxide then removed with a buffered HF solution.

Next, a second pad oxide (100 nm thick) is grown on the exposed recessed silicon, followed by a 100nm CVD nitride that conformally covers all surfaces. These two layers are then anisotropically etched, which removes them from the bottom of the recessed silicon areas but not form under the overhanging nitride film. The second field oxide (2 um thick) is grown using high pressure oxidation at 900^0 C.

Figure 8 shows the spot isolation structure compared to the structures obtained with semi-recessed and fully recessed LOCOS. Because the shape of the exposed silicon following removal of the first field oxide is very smooth only small stresses are created between the silicon and SiO_2 as the second field oxide is grown. Hence, dislocation generation is avoiding [6].

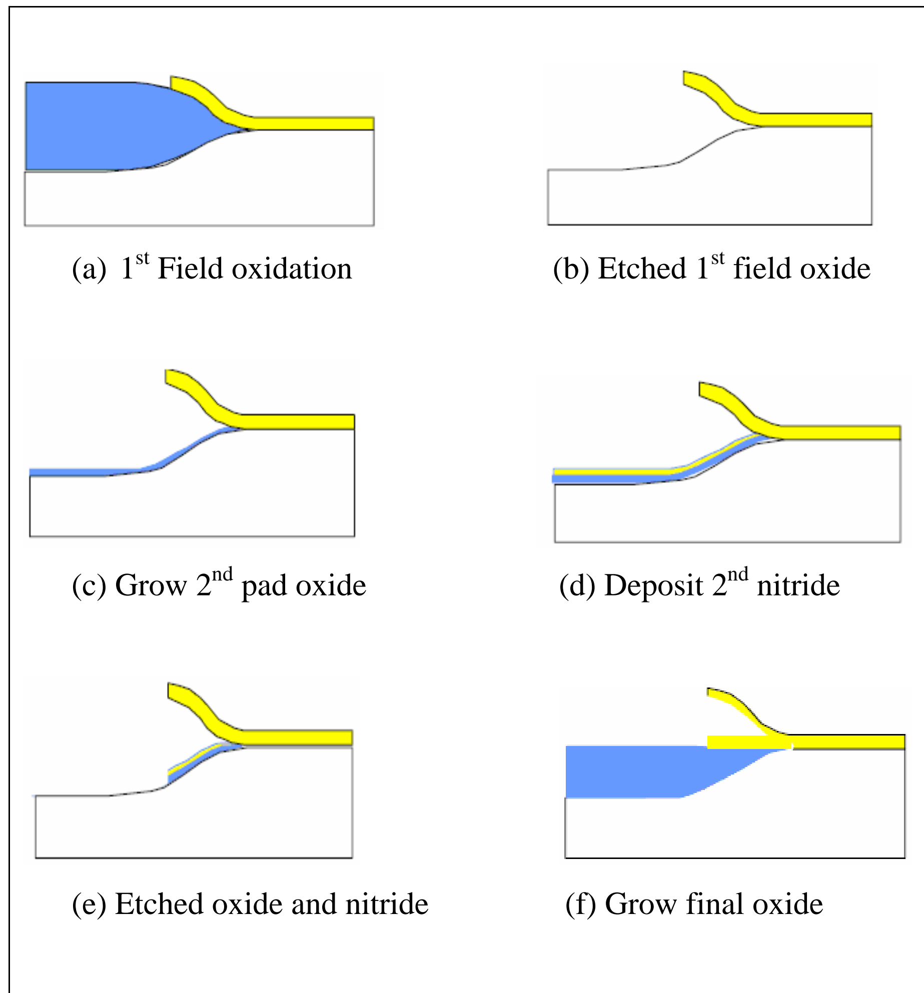


Figure 2.5: Cross section for Self-aligned planar-oxidation technology (SPOT) [6].

2.4.3 Fully recessed-oxide (FUROX)

The fully recessed-oxide (FUROX) isolation technology is very similar to the SPOT process just described, except that a nitridized oxide is used instead of using pad oxide to seal the silicon surface during growth of the oxide that form the recessed in the silicon substrate. This, there is less oxide encroachment into the active-device regions.

A thermal-oxide layer of 20 nm thickness is grown and is then nitridized in a NH ambient at 1200^0 C for seven hours. This provides a pad layer consisting of nitridized oxide that is capable of shutting of the diffusion path along the interface, with only a slight loss of the pad-oxide viscosity. The first LPCVD-nitride layer of 80-nm thickness and an undoped CVD oxide of 20-nm thickness are then deposited and patterned by means of plasma etching. The exposed nitridized oxide under the CVD nitride is etched away in a hot phosphoric bath. At this point the first field oxide is grown (450 nm thick), with the bird's beak largely suppressed by the nitridation-enhanced sealing ability. This field oxide is then chemically etched away to provide a moat of well-controlled depth and sidewall angle. The silicon surface is tree of dry-etch damage and has short nitride overhang.

A second pad-oxide layer (10 nm) is then grown and covered with a second CVD nitride (40 nm thick). After the self-aligned boron channel-stop implant is performed, the second nitride layer is etched anistropically, so that it still remains on the sidewall for oxidation masking. After the second field oxide has been grown, a defect-free, near-zero bird's beak, fully recessed oxide is produced with fairly good planarity. The narrow-width effects observed in conventional LOCOS are also reported to be significantly reduced [7]. All these process are shown in Figure 2.6.

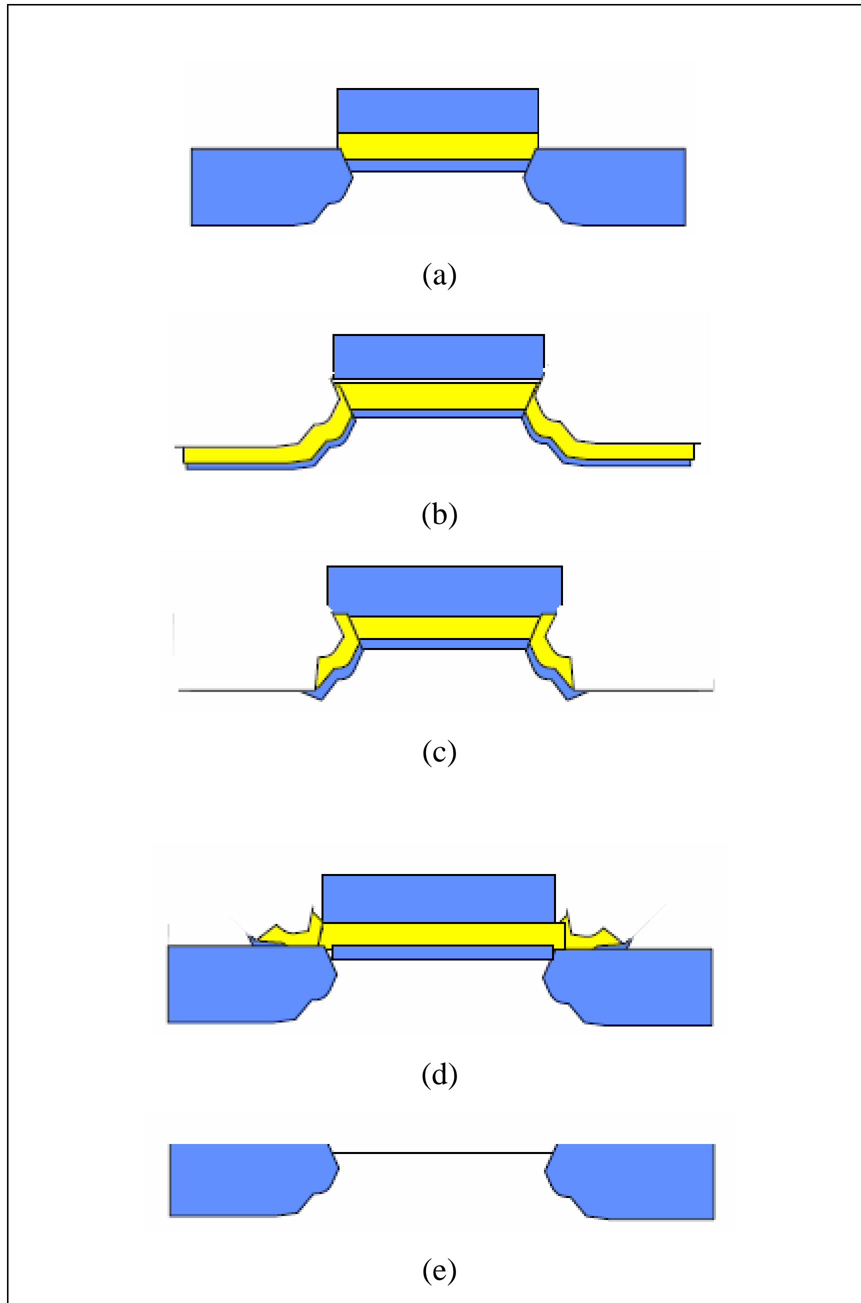


Figure 2.6: Cross section for fully recessed-oxide (FUROX) [7].

2.5 Locos problem

2.5.1 Stress damage

The stress can be large enough to cause damage in the silicon at the edge of the LOCOS. The source and drain junctions are also located at the edge of the LOCOS. The result is that the junctions are leaky. Stress increases with increased nitride thickness, increased field oxide thickness and decreased pad oxide thickness. In the RIT P-well CMOS process pad oxide is 500 Å, nitride is 1500 Å and field oxide is 11,000 Å. We may get more reliable results by decreasing the nitride to 1000 Å and decreasing the field oxide to 8000 Å [7]. The stress damage is illustrated in Figure 2.7.

Figure 2.7: Stress damage in silicon substrate [7].

2.6 Bird's beak suppression in LOCOS by mask-stack engineering

When isolation spacing approach 1 micron in dimension some other effects can be exploited to suppress lateral-oxide encroachment in a semi-recessed LOCOS process. First, the stiffness of the mask stack is dramatically increased, and as a result it exhibits much more resistance to bending as the oxide film grows laterally under it, than when the mask is wider. If the deformation of the mask stack can be decreased, lateral oxidation is also reduced since the oxide growth requires volumetric expansion. The magnitude of the lateral encroachment can be reduced by as much as 30% for a 0.5 um mask length, compare to along mask length. Through optimization of the relative film thickness of the mask stack,

along with the mask length and the degree of interface sealing, an acceptable degree of suppression of the bird's beak can be produces for a given technology.

2.7 Latest isolation technology

2.7.1 Shallow trench isolation

Shallow Trench Isolation is a device isolation technique for integrated circuits. As the semiconductor industry moves to sub 0.25 um CMOS technology there is a need for creating very small void free gaps on the wafer sub-layer. LOCOS was used before STI came into the picture. The STI creation process could be described in several step starting from oxidation, deposition of CVD silicon nitride, lithography, etching, cleaning process, fill and end with chemical mechanical planarization. Beside that, shallow trench isolation (STI) is a mainstream isolation method for advanced logic, mixed-signal, DRAM and other memory devices. Shrinking features and the LOCOS to STI transition have increased requirements for stringent process control. From this perspective, challenges lie in providing void-free, seamless gap fill, especially for high-aspect-ratio trenches, and CMP uniformity.

Traditionally, shallow trench characterization has been done using slower and localized techniques such as atomic force microscopy (AFM) or destructive methods such as scanning electron microscopy (SEM). These techniques yield information, but generally do not accommodate high-throughput sampling. Under certain circumstances, they may not lend themselves to wafer uniformity studies and can be difficult to apply in manufacturing environments. Etch depth control across wafer is critical in trench etch. Because it is a blind etch-and uniformity of fill and CMP depend on trench uniformity-trench depth control is crucial. In situ metrology capable of providing rapid feedback on trench depth and uniformity could be useful, minimizing test wafers and scrap. The design rule for n+ to p+ spacing is much larger than the n+ to n+ spacing rule due to the fact that the well isolation region has to support a well boundary and lithography misalignment of the active regions to the well boundary. This fact has stimulated the development of shallow and deep trench-based isolation approaches for device and well isolation respectively.