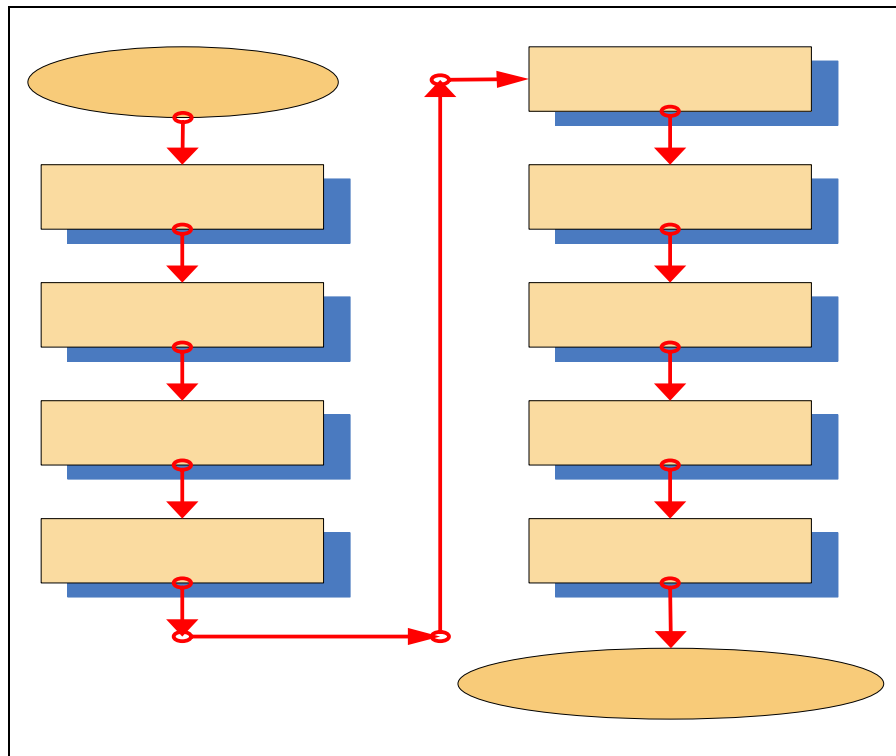


## CHAPTER 3

### METHODOLOGY

#### 3.1 Fully-recessed LOCOS

Fully recessed LOCOS is one of the conventional isolation technique which is has been invented to replacing the semi-recessed LOCOS. This technique shows that the better result is obtained compare with the semi-recessed LOCOS. The fully-recessed LOCOS comprising several steps which is shown below as Figure 3.0.

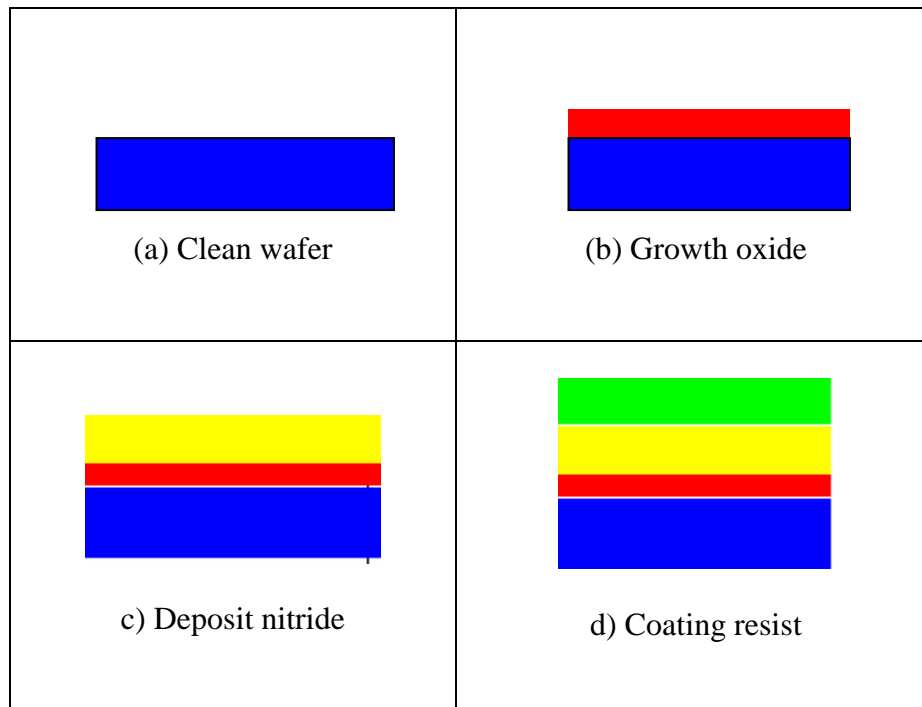


**Figure 3.0:** Flow chart for fully recessed LOCOS

### 3.2 Process flow for fully recessed LOCOS

A fabrication method to form fully recessed LOCOS, comprising the several steps. Firstly, providing a silicon substrate which includes at least one substantially monolithic body of silicon either p-type or n-type substrate. Then the wafer undergoes to cleaning process refer to Figure 3.1(a) using RCA-1 solution composition of  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  with 1:5:5 to 1:2:7 ratio at 70 C to 80 C to remove contamination and organic contamination and oxide etch using buffered oxide etch (BOE) to remove native oxide. After the RCA-1, wafers are rinsed by deionized (DI) water in a wet bench and dried in a spin dryer. Forming a pad layer of silicon dioxide over the silicon surface refer to Figure 3.1(b) using the dry oxidation with temperature about 900<sup>0</sup> C and the thickness of pad oxide is approximately 300 Å. Time to growth the pad oxide took about 1 hour process. The other method to growth the oxide layer is using wet oxidation. Wet oxidation is significantly faster than dry oxidation.

After that, deposit an oxidation-resistant layer of silicon nitride refer to Figure 3.1(c) using plasma enhanced chemical vapor deposition (PECVD) and thickness of the nitride layer is approximately 2000 Å after measured using spectrophotometer. The time process for deposited the nitride layer is 8 minutes over said pad oxide layer. Typically this nitride is not directly deposited on silicon, but overlies a thin oxide layer. This nitride and oxide layer (which may include additional layers) is often referred to as the active stack. Then the wafer is placed to the photolithography process to determine the first pattern as a Figure 3.1 (d). First, coating a positive resist over the entire wafer surface using a spinner. After coating resist the wafer is undergo soft bake to produce the adhesion of resist over the nitride layer. Time to soft bake took about 60 second.



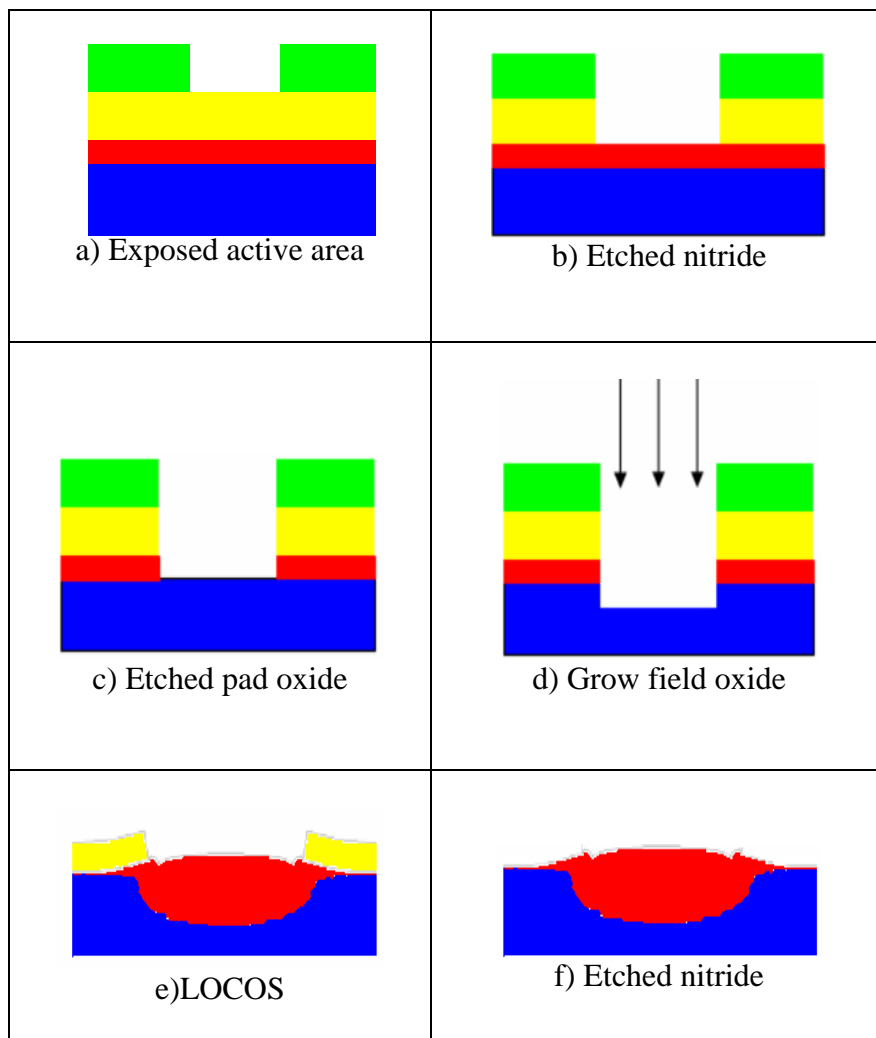
**Figure 3.1:** Standard process for fully-recessed LOCOS

After 60 second process completed the first pattern will determined using mask aligner. Time to expose the first pattern took about 110 second. The area which is not covered by pattern will be dissolved by the developer while the unexposed parts remain on the wafer surface. These occurred because, for the positive photoresist, the main component is novolac resin, which is cross-linked polymer before the exposure. After the exposure process, the exposed part's cross links break down and become "softened" due to the photochemical reaction called photosolubilization, and will be solved by the developer as shown in Figure 3.2 (a).

The process continues with the dry etched nitride using reactive ion etch (RIE). The time process took about 3 minutes as shown in Figure 3.2 (b). The etch rate for nitride layer is  $650 \text{ \AA} / \text{min}$ . There are two types of etching process. One is wet etching that uses chemical solution to dissolve the materials on the wafer surface to achieve the devices and circuit requirements. Wet etch normally has very good selectivity and a high etch rate, which is mainly controlled by the etchant temperature and concentration. Hot phosphoric acid is most commonly used to etch silicon nitride. At  $180^\circ \text{C}$  with 90 %  $\text{H}_3\text{PO}_4$  concentration, the nitride etch rate is about  $100 \text{ \AA} / \text{min}$ . This nitride etch process has very good selectivity to thermally grown silicon dioxide and to silicon. Increasing  $\text{H}_3\text{PO}_4$  concentration to 94 % and temperature  $200^\circ \text{C}$ , increase the nitride etch rate to  $200 \text{ \AA} / \text{min}$ . Selectivity to silicon dioxide drops to about 1% and selectivity to silicon reduces to around 20:1.

Then the process continued with etching pad oxide using buffered oxide etches (BOE). Etch rate for oxide etch using buffered oxide etch is approximately  $400 \text{ \AA} / \text{min}$ . Time to implement the oxide etch is about 90 seconds which is needed high concentration because buffered oxide etch is fast etchant in room temperature, it is difficult to control the oxide etch process as shown below in Figure 3.2 (c). After the pad oxide has been removed the process continued to etch the silicon. There are two methods to etch silicon either dry etching or wet etching. The process for dry etching is much better compared with the wet etching. Reactive ion etch is used to etch the unwanted silicon as illustrated in Figure 3.2 (d). The time to etch silicon using reactive ion etch is about 2 minutes process. For wet etching the profile is isotropically with a mixture of nitric acid ( $\text{HNO}_3$ ) and hydrofluoric acid (HF). It is a complex chemical reaction. First,  $\text{HNO}_3$  oxidizes the silicon on the surface to form a thin layer of silicon dioxide, which can block the oxidation process. HF then reacts with silicon dioxide and dissolves it, exposing the silicon underneath, which is oxidized again by  $\text{HNO}_3$ . Then the oxide is again etched away by the HF. The process repeats again and again. Then growth field oxidation as illustrated below in Figure 3.2 (d) by using a wet oxidation.

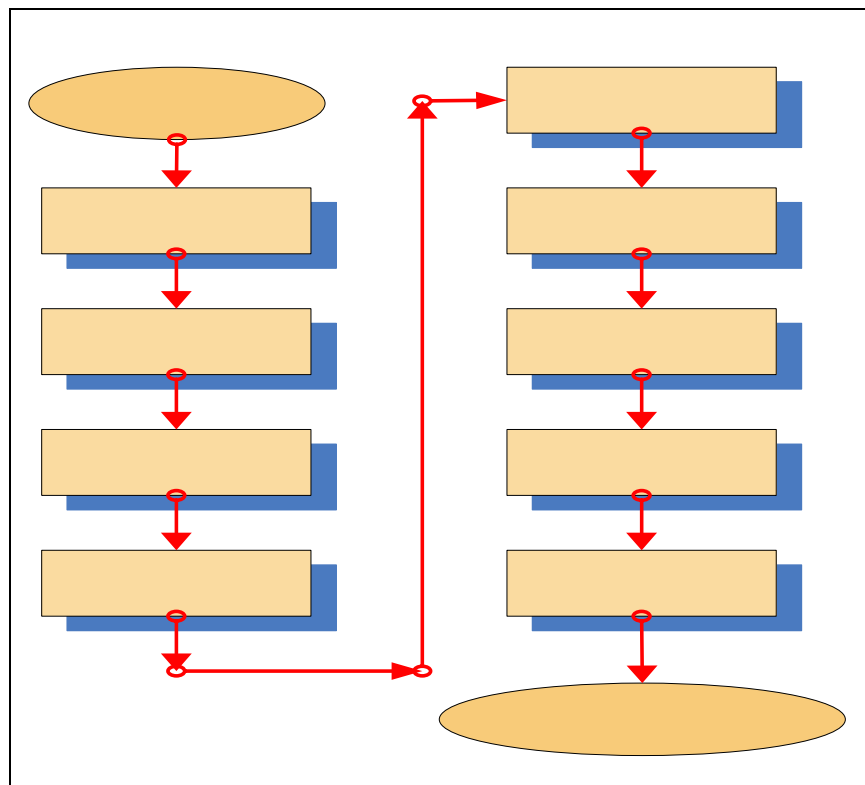
The time process for wet oxidation is about 1 hour 30 minutes with temperature around  $1000^{\circ}\text{C}$  and the target thickness is range  $4000\text{ \AA}$  to  $5000\text{ \AA}$ . After finished the field oxidation then, measure the wafer thickness using spectrophotometer to measure the thickness of oxide. The oxide will oxidizes at the top of nitride layer which is can associate the problem. So, the oxide on the top of nitride layer should be etch using a buffered oxide etch (BOE). Finally the nitride layer will be etch using reactive ion etch which is time process took about 3 minutes for  $2000\text{ \AA}$ . Etch rate for nitride layer using reactive ion etch is about  $600\text{ \AA}/\text{min}$  and the recipe for the etch process is 45 % for  $\text{CF}_4$  and 5 % for nitrogen gases.



**Figure 3.2:** Process flow for fully-recessed LOCOS

### 3.3 Poly Buffered LOCOS

Among many isolation schemes that have been tried to reduce the bird's beak encroachment, poly buffered LOCOS (PBL) appears to be the most widely adopted LOCOS-based structure for 0.8–0.5 micron CMOS technology since it was evolved from the well proven LOCOS process by simply inserting a polycrystalline silicon (polysilicon) layer. Poly buffered LOCOS (PBL) has emerged as the most likely advanced isolation technique to achieve the benefits of LOCOS without suffering excessive process complexity. PBL incorporates the use of a stress-relief polysilicon layer between the pad oxide and nitride. Process flow for poly buffered LOCOS is quite similar with the fully recessed LOCOS. Only the differences between two methods are for fully-recessed LOCOS there are no polysilicon layer that existed after grow pad oxide. Figure 3.3, shows a process flow for poly buffered LOCOS comprising several step which is start with the wafer thickness measurement and ended with Grow field oxide.

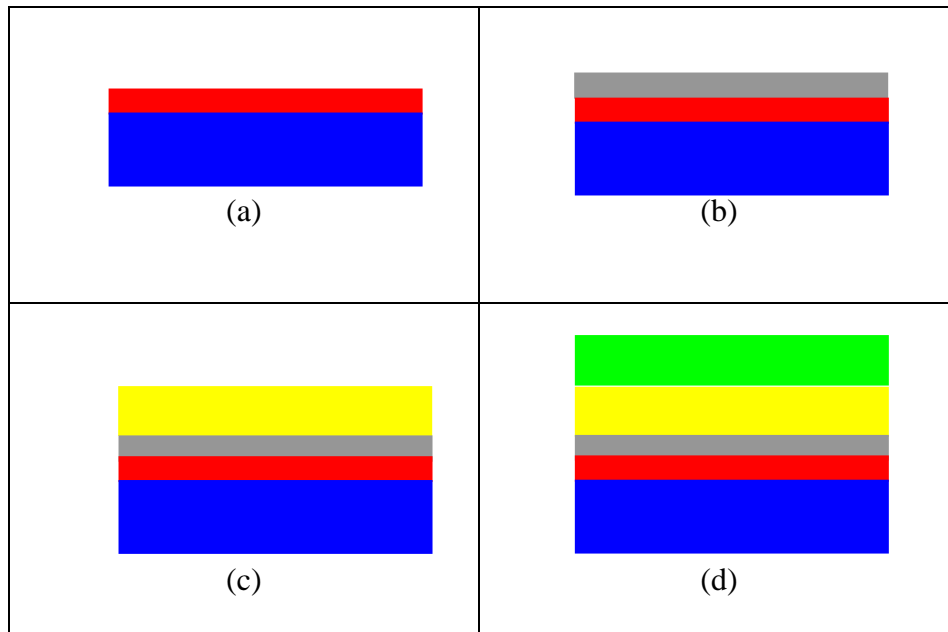


**Figure 3.3:** Flow chart for poly buffered LOCOS

### 3.4 Process flow for poly-buffered LOCOS part 1

Figure 3.4 shows a schematic process sequences for poly-buffered LOCOS. The process starts with the wafer thickness measurement and then continues with cleaning process using RCA-1 to eliminate the particle and contamination in the wafer surface. First, thin thermal oxide (400 Å) was grown as the stress relief oxide or pad oxide as shown in Figure 3.4 (a) using dry oxidation. The process then, followed by plasma enhanced chemical vapor deposition (PECVD) of amorphous silicon and the thickness of the amorphous is 500 Å and thereafter PECVD silicon nitride ( $\text{Si}_3\text{N}_4$ ) and the thickness is 2000 Å were deposited, respectively as illustrated in Figure 3.4 (b) and (c). After that, the sample is undergoing to lithograph process. The process of lithography includes several steps which are consisting of coating resist using spinner. During the coating resist process the program M have been chosen with the ramp –up setting is 1000 second and ramp-down setting is 50 second.

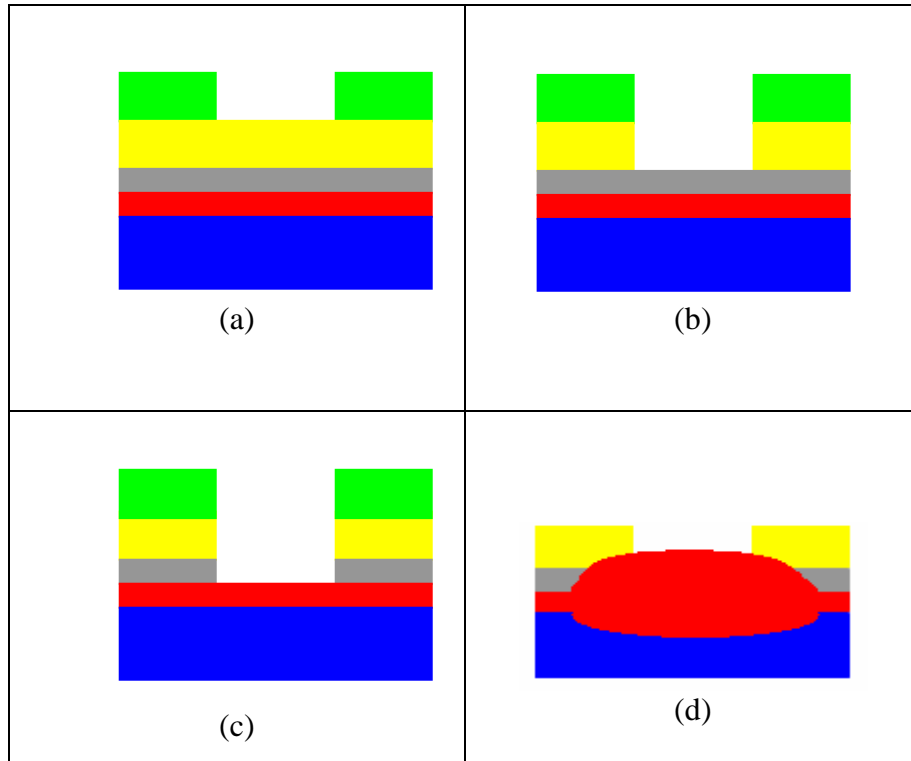
The process then, followed by soft bake using a hot plate. Time to soft bake took about 60 second. Then sample is placed into mask aligner to transfer the active area pattern. The time exposed during pattern transfer is around 110 second. The process followed by hard baked which is took about 1 minute process using a hot plate and then, the pattern is determined using a developer. This process should take some precaution to protect the sample from over develop or incomplete develop. The time taken during develop process is around 3 to 4 minutes.



**Figure 3.4:** Process sequences for Poly-buffered LOCOS part 1

After photoresist mask formation, nitride and polysilicon were etched by reactive ion etch (RIE). The recipe for etching the nitride and poly layer using RIE is 45% for  $\text{CF}_4$  and 5 % for nitrogen gases and the process took about 3 minutes for 2000Å thickness of nitride and 6 minutes for 500 Å thickness of polysilicon. The depths of the shallow etching were in the range of 2300-2500 Å as shown in Figure 3.5 (a) and (b). Finally the field oxide of 4500 Å was thermally grown in the wide-open areas as illustrated in Figure 3.5 (d). Then the thickness of field oxidation is measured using spectrophotometer. After field oxidation there some oxide exists at the top of nitride layer. So, it should be etched using a buffered oxide etch (BOE).





**Figure 3.5:** Process sequences for poly-buffered LOCOS part 2

