CHAPTER 3

METHODOLOGY

3.0 Overview

This chapter provides methodology of process fabrication transistor and electroless NiAu at Unimap Cleanroom Lab. Basically to run experiment in cleanroom lab, most important thing is must have the run chart. The run chart is very important because it has all information such as schedule of process flow, parameter is using, chemical, time, temperature, etc. Any information, problem before and after experiment must be written in the run chart. For this project it can be divided into 3 sections, start will first design, fabrication and last section is an electrical characterization.

In this project, the several steps are introduced to fabricated transistor will be design mask, photolithography process to develop pattern for source and drain, gate, contact, metallization and lastly bonding pad.

AlNiAu as the interconnection involved of several steps. It start with Al deposition, the follow by cleaning, activation and zincation to remove the oxide layer thus, provide good adhesive. The next process is nickel deposition and lastly gold in deposited on top of Ni. Gold is used because of is not easily oxidize upon exposure for environment.

3.1 Process Fabrication transistor (nMOS and pMOS)

3.1.1 Mask Design

For this project AutoCAD software is used for design masks. Mask design is very important before fabrication process can be done. The whole transistor process has six masks steps and each mask have different size as shown in **Table 3.1**

Table 3.1 Mask and size of transistor.

Mask Pattern	Size(μm)
Mask 1 - Source/Drain	1000 x 1000
Mask 2 - Gate	90 x 1040
Mask 3 - Contact	500 x 500
Mask 4 - Metal	630 x 1460
Mask 5 - Passivation layer	4470 x 3540
Mask 6 - Bonding Pad	500 x 500

3.1.2 Wafer cleaning and filed oxidation

The wafer is chemically cleaned using BOE (buffered oxide etch) for 1 minute and followed by De-ionized water rinse and spin dry processes. The purpose of wafer cleaning is to remove particulate matter on the surface as well as any traces of organic, ionic, and metallic impurities**.** The next step is oxidation process, there are two SiO_2 growth methods, dry and wet oxidation, depending on whether dry oxygen or water vapor is used. Dry oxidation is usually used to form thin oxides in a devices structure because of its good Si-SiO_2 interface characteristics, whereas wet oxidation is used for thicker layer because of its higher growth rate.

The wet oxidation is carried out to form a uniform and pure silicon oxide layer for the next diffusion process. The silicon oxide will be where the source and drain mask design will be transferred to. Then, etch will be carried out to form wells that allows diffusion, and process parameter wet oxidation are show below **Table 3.2**. After the wet oxidation process, a SiO_2 layer is formed all over the wafer surface as show in **Figure 3.1 (c),** and oxide thickness is measured using spectrophotometer.

The reaction can be expressed as:

$$Si\ (solid) + 2H_2O\ (vapor) \longrightarrow SiO_2\ (solid) + 2H_2\ (vapor) \qquad (3.1)$$

Table 3.2 Process Parameter for Wet Oxidation.

Method oxidation	Wet oxidation
Set up the furnace	Ramp-up : 500 ^{0}C Time : 1 hour Gas flow : O_2 = 1ℓ/m N_2 = 5ℓ/m Temperature : 1000 ^{0}C
Time Oxidation	60 minutes

3.1.3 Source/drain formation

After the formation of SiO_2, the wafer is coated with an ultraviolet (UV)-light-sensitive material called a photoresist as show in **Figure 3.1 (d)**, which is spun on the wafer surface by high-speed spinner. After spinner, the wafer is baked at about 90°C to drive the solvent out of resist and to harden the reisit for improved adhesion. **Figure 3.1 (e and f)**, shows the next step, which is to expose the wafer throught a patterned (mask 1) using an UV-light source. The exposed region of the photoresist-coated wafer undergoes a chemical reaction depending on the of resist. The exposed area to light become polymerized and difficult to remove in an enchant. The polymerized region remains when the wafer is placed in a developer, whereas the unexposed region (under the opaque area) dissolves and washes

away. **Figure 3.1 (g)** shows the wafer after the development. The wafer is again baked into hot plated to enhance the adhesion and improve the resistance to the subsequent etching process. Then, an etch using buffered oxide etch (BOE) removes the unprotected SiO_2, surface as show in **Figure 3.1 (h)**. **Figure 3.1** shows the final result of a region without oxide (a window) after the lithography process and **Table 3.3** show the process parameter for lithography process.

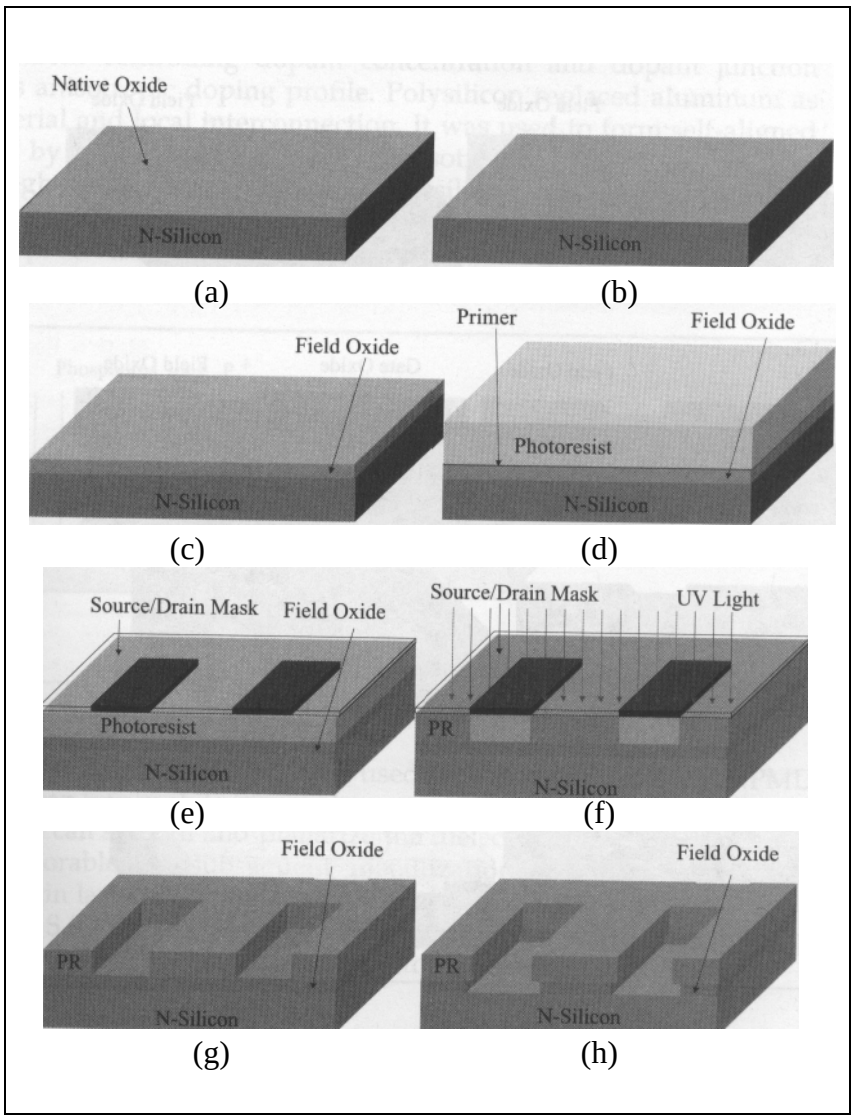


Figure 3.1 Fabrication Process step (a) and (b) process wafer cleaning using BOE (Buffered Oxide Etch). (c) An oxidized Si wafer by wet oxidation. (d) Application of resist. (e) and (f) Resist exposure through the mask. (g) The wafer after the development. (h) The wafer after SiO_2 removal.

Table 3.3 Process Parameter for lithography process.

Process	**Paramater**
Spin Spinner	Ramp-up : 800 rpm (5 second) Speed : 3000 rpm(10 second) 0 rpm (5 second) Time : 20 second
Resist	Positive Resist
Soft bake	Time : 90 second Temperature : 90 °C
Exposure	Light source : Fluorescent Time : 110 second
Hard bake	Time : 60 second Temperature : 90°C

Figure 3.2 (a) show the resist are stipped away using acetone. The wafer is then ready for forming the *p-n* junction by a diffusion process. The wafer is placed in a furnace with gas containing the dopants. When heated, dopant atoms diffuse into substrate. First step, dopant liquid (*boron / phosphorous*) will deposit on surface wafer using spin spinner, heat the sample into hot plate at 90 °C until 90 second. After that, the sample load into furnace for drive-in process. Lastly immerse the wafer into BOE solution as show in **Figure 3.2 (b)**, and measure sheet resistance using DCM 40515-Vi software and **Table 3.4** show that process parameter for this process.

Table 3.4 Process Parameter for diffusion process.

Process	**Paramater**
Dopant liquid	Boron – (doped n^+ for nMOS) Phosphorous – (doped p^+ for pMOS)
Spin Spinner	Ramp-up : 1000 rpm (5 second) Speed : 3000 rpm(10 second) 0 rpm (5 second) Time : 20 second
Soft bake	Time : 90 second Temperature : 90 °C
Set up the furnace	Ramp-up : 500 ^{0}C Time : 1 hour Gas flow : O_2 = 1ℓ/m N_2 = 5ℓ/m Temperature : 1000 ^{0}C

3.1.4 Gate formation

For gate formation the process are same as the source/drain formation but it use different mask (mask 2). After done process lithography process, a very thin gate oxide (a few hundred angstroms) is grown by thermal oxidation/dry oxidation and measure oxide thickness as shown in **Figure 3.2 (c and d)**. **Table 3.5** show that process parameter for gate oxidation using dry oxidation method.

Table 3.5 Process Parameter for Dry Oxidation.

Method oxidation	Dry oxidation
Set up the furnace	Ramp-up : 500 ^{0}C Time : 1 hour Gas flow : O_2 = 1ℓ/m N_2 = 5ℓ/m Temperature : 1000 ^{0}C
Time Oxidation	30 minutes

3.1.5 Contact formation

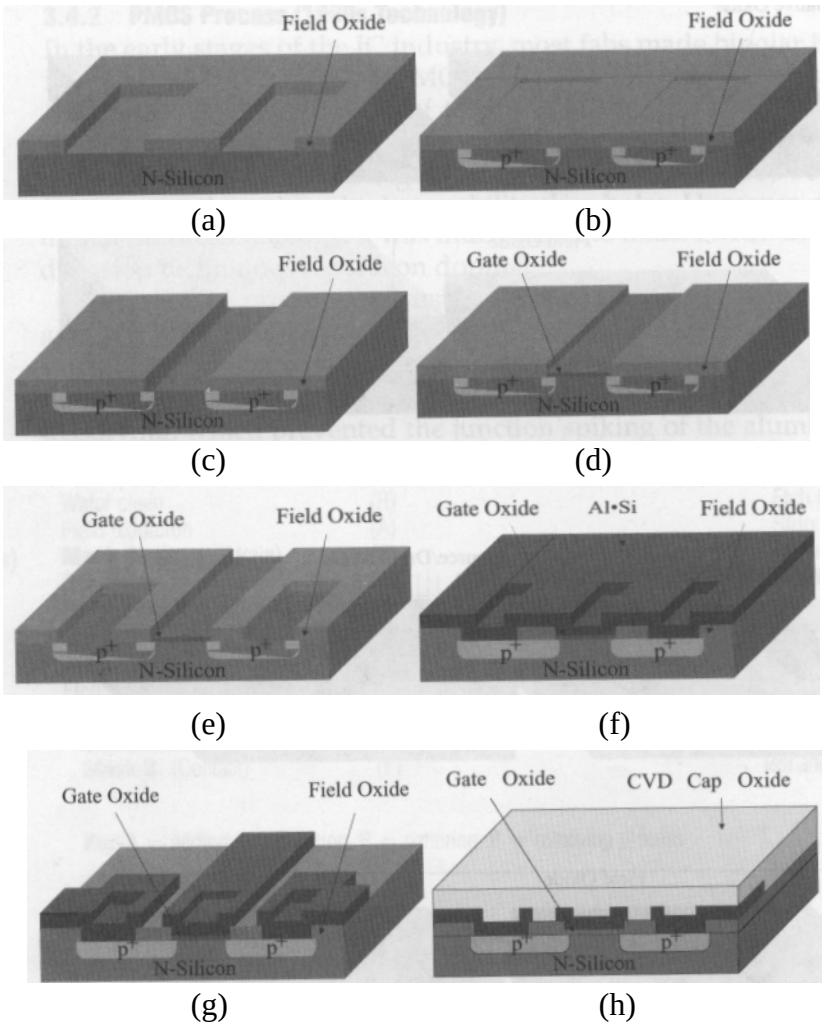
Same as gate formation process, mask 3 is used to form contact on this sample. After lithography process (deposit photoresist, soft bake, UV exposure, develop, hard bake, strip photoresist) the following next step is deposit aluminum into contact area**. Figure 3.2 (e),** show the contact pattern (source, drain and gate) on the surface sample. Generally contact is use to form space/area on active area (source, drain and gate) before deposited aluminum for interconnection between three terminal with external connection such as wire bond.

3.1.6 Metallization formation

After contact formation process, a metallization process is used to form ohmic contacts and interconnections. Metal films (aluminum) can be formed by physical vapor deposition **(Figure 3.2 f).** The lithography process is again used to define the front contact which is shown in **Figure 3.2 (g)**. A similar metallization step is done on the back contact about using a lithography process.

3.1.7 Bonding Pad Formation

Bonding pad is a pad base connection between internal terminal (source,drain and gate) to external connection such as wire bond for providing electrical. To make a bond pad, firstly the sample will deposited silicon oxide or silicon nitride to protect the device for contamination and it called passivation layer. **(Figure 3.2 h)**



Continue: Figure 3.2 Fabrication pocess step (a) after strip photoresist using acetone. (b) source/drain doping. (c) Form gate pattern using lithography process. (d) Grown gate oxide using dry oxidation. (e) Form contact pattern (f) deposit metal (aluminum) using PVD. (g) After aluminum etch. (h) Deposited passivation layer.

3.2 AlNiAu Process Using Electroless UBM Method

Figure 3.3 shows that process flow of electroless nickel immersion gold deposition on Al bond pad. Firstly the bare wafer will be cleaning process using BOE for remove any contamination such as native oxide before aluminum deposition. After done form bonding pad, the wafer will be grow silicon nitride for passivation layer using PECVD. The following next process is chemical preparation for deposited Ni and Au layer into aluminum bond pad **Table 3.6**, and for deposited Ni and Au the process flow is surface cleaning, aluminum bond pad activation, first zincation, zinc removal, second zincation, electroless nickel, and lastly immersion gold.

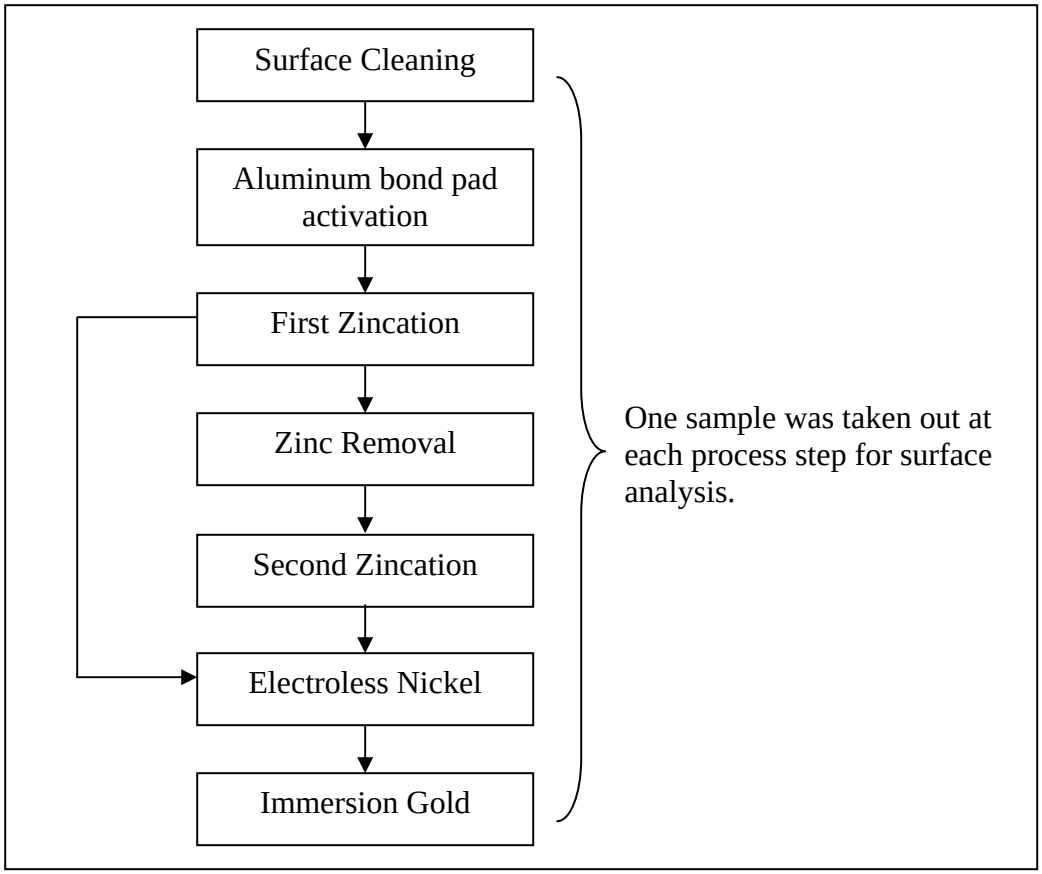


Figure 3.3. Process sequence for electroless nickel immersion gold deposition.

3.2.1 Bond Pad Aluminum

In this experiment aluminum foil will be deposited using evaporated method (PVD) on the wafer and then patterned using photolithography using a bond pad mask. Thickness aluminum must be in range 1 µm ~ 2 µm, if aluminum less than 1 µm after remove zincation process all aluminum layer will be remove (bare wafer).

3.2.2 Deposit Passivation Layer

Passivation layer is used to protect surface silicon to contamination. Silicon nitride will be deposited on the surface wafer using PECVD Thickness silicon nitride about 5000Å, the next step is remove silicon nitride on aluminum bond pad using mask 2. RIE is used for remove silicon nitride after develop pattern using photolithography. The completed process is show in **Figure 3.4.**

3.2.3 Deposit Photoresist Layer

Photoresist will be deposited on silicon nitride to protect this layer during electroless nickel process. Thickness of photoresist layer is 2 µm.

3.2.4 Chemical Preparation

The chemical used in this experiment is newly prepared solution. Process parameters and make-up solution was shown in **Table 3.6.**

Table 3.6 Make-up solution and process parameters

No.	Process	Make-up	Parameter
1	Cleaning	Ready to use solution	3 min,71 °C
2	Activation	Ready to use solution	1 min, RT
3	First zincation	50%zincate,50%De-ionized water	1 min, RT
4	Zinc removal	Ready to use solution	30 sec,RT
5	Second zincation	50% zincate, 50% De-ionized water	1 min,RT
6	Electroless nickel	76.92% De-ionized water, 15.38% Ni200 Make-up, 6.15% Ni200 Replenisher A,	30 min, 80 °C ~ 85 °C
7	Immersion gold	64.45% De-ionized water, 30.26% Au200 Make-Up, 1% Au Salt	5 min, 85 °C
RT: room temperature; The percentages (%) shown in table are by volume.			

3.2.5 Surface cleaning

Cleaning process is cleaned aluminum pads were micro-etched to remove soft aluminum oxide and activated for better nucleation at subsequent process an also to performed to remove various contaminations that were presents on the wafer surfaces that were due to material handling. The sample immersing by cleaner until 3 minutes at 75 °C after that rinse with de-ionized water until 1 minute.

3.2.6 Aluminum bond pad activation

The purposes of activation process are to micro-etch the aluminum oxide and activate the surface for better nucleation at subsequent process. The sample immersing by activator until 1 minute at room temperature and rinse with de-ionized water until 1 minute.

3.2.7 First Zincation

The zincation is a process of coating the aluminum bond pad with a layer of zinc. The zinc layer will prevent the re-oxidation on aluminum bond pad and to initiate the electroless nickel deposition [19]. During the zincation process the aluminum oxide completely dissolved into solution while depositing zinc-nickel on the surface. This reaction is given as shown in below formulation. The general formulations during zincation are given as below. The first zincation process was done by immersing the dice into zincation solution until 1 minute at room temperature and rinsed with de-ionized water to avoid chemical mixture to the subsequent process until 1 minute.

Aluminum bond pad oxide elimination through:

$Al_2O_3 + 6NaOH \rightarrow 2Al(OH)_3 + 3Na_2O$

Zinc and Nickel through displacement reaction:

$3\ Zn^{2+} + 2\ Al \rightarrow 3\ Zn + 2\ Al^{3+}$

$3\ Ni^{2+} + 2\ Al \rightarrow 3\ Ni + 2\ Al^{3+}$

3.2.8 Zinc removal

At this process the first zinc and nickel layer was removed using the selective etching of nitric acid. The sample immersing by zinc removal until 30second at room temperature and rinse with de-ionized water until 1 minute. Generally nitric acid attacks all the base metals except aluminum, therefore makes it suitable for removing zinc and nickel on the aluminum bond pad surface.

3.2.9 Second zincation

Second zincation is a common preferred method for plating aluminum and is especially useful on certain difficult-to-plate alloys to ensure better adhesion of the final metal layer deposit. Zincation treatment is applied on Al bond pads in order to activate the Al surfaces for the adhesion of electroless Ni. The properties of the metal plate are directly related to the thickness, uniformity and continuity of the zincates coating with thinner coating generally providing smoother and more adhesive metal plating [20]. The second zincation was done after removing the zinc on the surface through wet etches and process step are immersing by zincation solution until 1 minute at room temperature after that rinse with de-ionized water until 1 minutes.

3.2.10 Electroless Nickel.

The samples were then dipped into the electroless nickel solution until 30minutes at temperature 80 °C ~ 85 °C after that rinse with de-ionized water until 1 minutes. Zinc that was used to initiate the reaction was dissolved in the electroless nickel solution during the reaction with ion zinc as following equation:

Reduction: $Ni^{2+} + 2^{e-} \rightarrow Ni$ (3.2)

Oxidation: $Zn \rightarrow Zn^{2+} + 2^{e-}$ (3.3)

General formulation of electroless Ni (P) deposition.

$Ni^{2+} + H_2O + NaH_2PO_2 \rightarrow Ni(P) + H_2 + NaH_2PO_3B$ (3.4)

3.2.11 Immersion Gold

When electroless nickel deposition was completed, next step is immersion gold at temperature 85 °C until 5 minute after that the sample rinse with de-ionized water. The

deposition of gold layer was carried out to prevent the surface from oxidation and improves solderability. The gold layer coating mechanism is involves exchange reaction occurring between gold ion and nickel known as an immersion process. An immersion process referred to as displacement or replacement processes, depends on the oxidation of the less noble metal surface to supply electrons for the reduction of the more noble metal from solution. In the case of electroless nickel/immersion gold, Au ions in the solution took electrons from Ni atoms because of their difference in galvanic potential. In theory, the process is self limiting, once the surface is covered with Au, the process will stops. Basically, the overall reaction displacement between Ni and Au in the process is presented as below:

$$2Au^{+} + Ni^{2} \rightarrow Au + Ni^{2+} \quad (3.5)$$

$$\text{Reduction: } Au^{+} + e^{-} \rightarrow Au \quad (3.6)$$

$$\text{Oxidation: } Ni \rightarrow Ni^{2+} + 2e^{-} \quad (3.7)$$

3.2.12 Strip Photoresist

After completed deposited immersion gold, the end of this process are remove resist layer using acetone solution. **Figure 3.3** below show that process steps AlNiAu interconnection using electroless Nickel method.

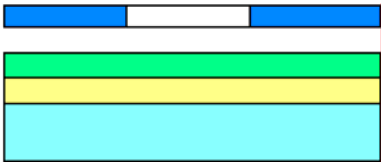
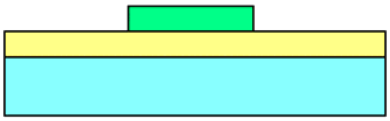
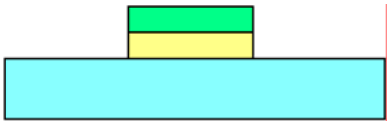
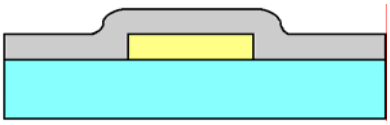
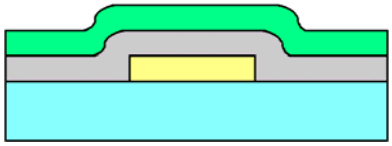
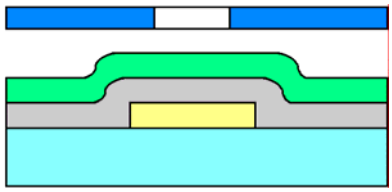
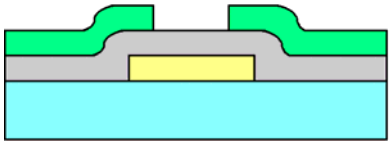
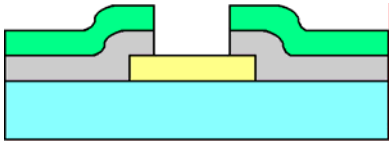
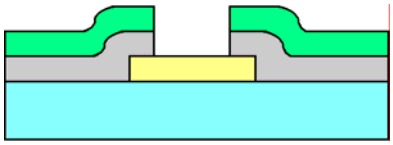
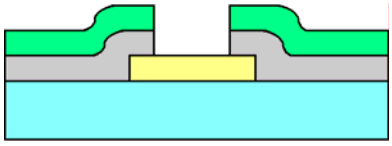
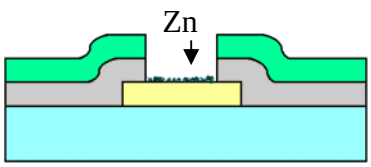
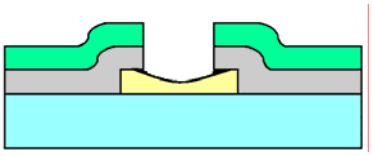
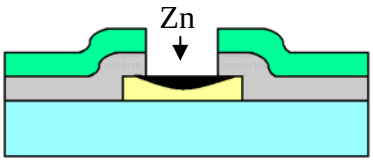
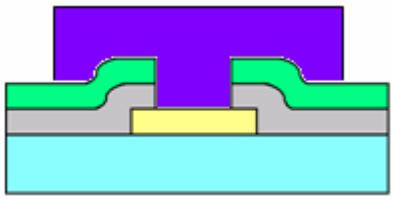
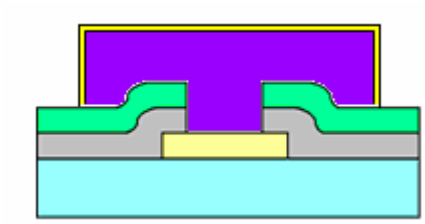
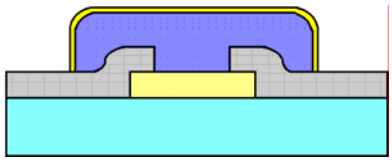
Process	Figure	Process description / parameter
1. Wafer cleaning		- A p-type (100) 4-16 ohms-cm silicon wafer is used as the sample substrate. - The process starts by cleaning the wafer using BOE cleaning method.
2. Aluminum deposition		- evaporated aluminum layer on the wafer using (PVD). - thickness (1µm ~ 2µm).
3. Photoresist coating		- deposited resist for pattern transfer (bond pad)
4. Alignment and expose		- mask 1 use during expose by UV light to form bond pad aluminum pattern.
5. Photoresist development Silicon wafer		- will be dissolved by the developer while the unexposed parts remain on the wafer surface.
6. Aluminum etch		- use aluminum etch solution to remove aluminum.
7. Photoresist removal		- remove resist using acetone solution.
8. Grow oxide		- grown oxide by PECVD for passivation layer.

Figure 3.4 Process flow of AlNiAu interconnection. Deposition oxide layer, continue:.

9. Photoresist coating		- to form pattern on silicon oxide layer.
10. Alignment and expose		- mask 2 use during expose by UV light to form pattern.
11. Photoresist development		- will be dissolved by the developer while the unexposed parts remain on the wafer surface.
12. Etch oxide		- use BOE solution to remove oxide layer.
13. Surface cleaning		- cleaned aluminum pads to remove soft aluminum oxide and activated for better nucleation at subsequent process. - temp. 75°C, 3 min. - rinse de-ionized 1min.
14.Aluminum bond pad activation		- activation process are to micro-etch the aluminum oxide and activate the surface for better nucleation at subsequent process. - room temp. 1 min. - rinse de-ionized 1min.

Continue :. **Figure 3.4** Process of develop Al bond pad until activation process. Continue

15. First zincation		- process of coating the aluminum bond pad with a layer of zinc. - room temp. 1 min. - rinse de-ionized 1min.
16. Zinc removal		- nickel layer was removed using the selective etching of nitric acid. - room temp. 30sec - rinse de-ionized 1min.
17. Second zincation		- activate the Al surfaces for the adhesion of electroless Ni. - room temp. 1 min. - rinse de-ionized 1min.
18 Electroless nickel		- deposited nickel using electroless method. - temp. 80°C ~ 85°C, time 30min. - rinse de-ionized 1min.
19. Immersion gold		- the deposition of gold layer was carried out to prevent the surface from oxidation and improves solderability. - temp. 85°C , 5 min. - rinse de-ionized 1min.
20. Photoresit removal		- remove/ strip resist on passivation layer. - use acetone solution.

Continue:. **Figure 3.4** Completed process of electroless nickel immersion gold deposition on Al bond pad.