

CHAPTER 4

RESULTS AND DISCUSSION

4.0 Overview

During the fabrication process of transistor, the problem is hardly to develop contact into surface wafer. During lithography process to develop the contact, the pattern cannot be form after immersion into developer solution. It is because quality of mask not very compatible to develop the smaller size.

Scanning Electron Microscope (SEM) was used to obtain the surface morphology; Energy Disperse XRay (EDX) for elemental analysis and Atomic Force Microscopy (AFM) for surface topographic. The average surface roughness was carried out over an area selected with the aid of a cursor on the display screen using Atomic Force Microscopy (AFM). The surface roughness of first and second zincation was compared using Atomic Force Microscopy (AFM).

4.1 Process fabrication of transistor

In this process involved several process steps, first mask design, photolithography process, oxidation, diffusion and lastly metallization. Photolithography is the patterning process that transfers the designed pattern (source/drain, gate, contact, metal, and bonding pad) from the mask to the photoresist on the wafer surface. Oxidation is used for development high-quality silicon dioxide (SiO_2) as an insulator or mask for diffusion process. For example dry oxidation is usually used to form thin oxide in the device for interface characteristics between Si- SiO_2 . But wet oxidation is used for thicker layers because of its higher growth rate and made it as a mask for diffusion process.

For a pMOS, the substrate is n-type, and the source/drain are heavily p-type doped such as boron, and for an nMOS, the substrate is p-type, and will deposited phosphorous (n-type). After diffusion process, a metallization process is used to form ohmic contacts and interconnections. Metal film such as Aluminium can be formed by physical vapour deposition.

4.1.1 Mask Design

Mask design is very important before fabrication process can be done. **Figure 4.1** show the layout of transistor, the whole transistor process has six mask steps and each mask have different size. Distance between source and drain are measured as a gate length, in this design, gate length each transistor is $50\ \mu\text{m}$. The whole transistor (pMOS and nMOS) process has six mask (source and drain, gate, contact, metallization, passivation and bonding pad) steps as show in **Figure 4.2**.

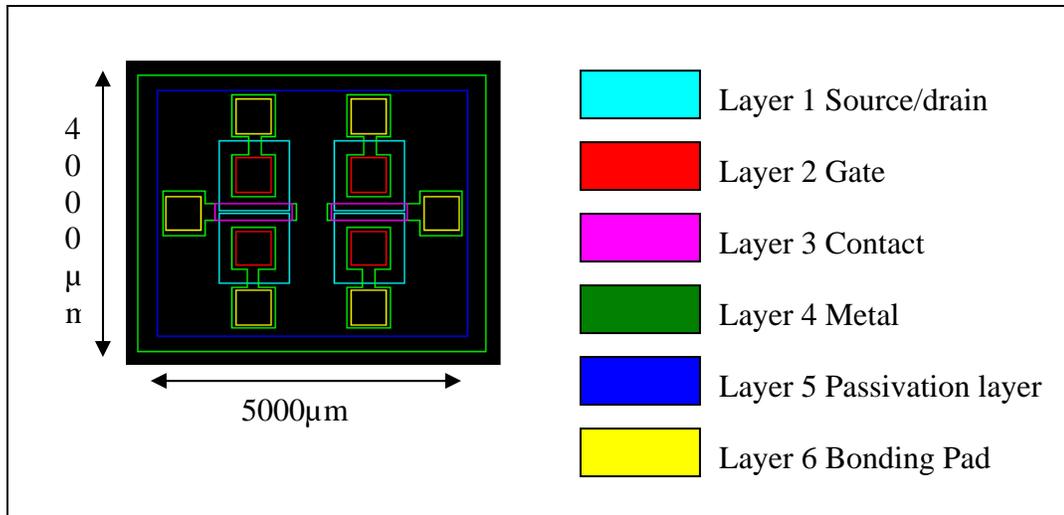


Figure 4.1 : Masking, a) Source/drain, b) Gate, c) Contact, d) Metallization, e) Passivation layer, f) Bonding pad.

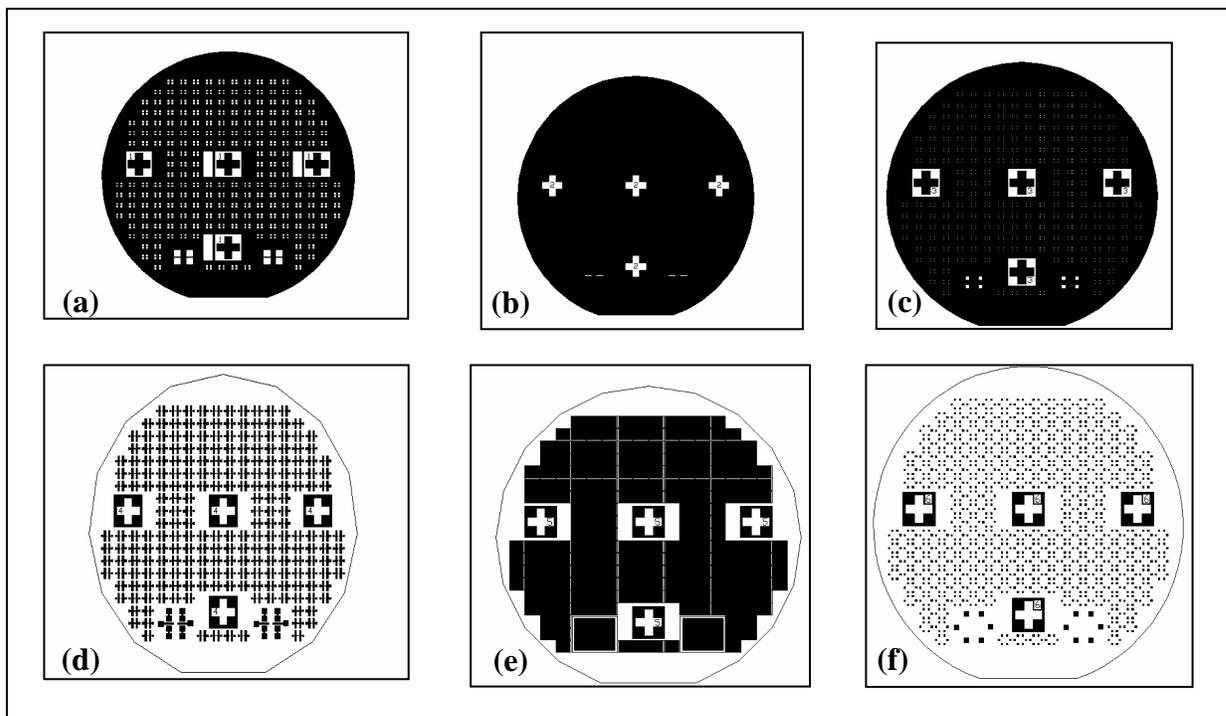
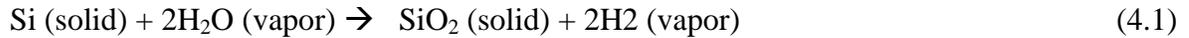


Figure 4.2 : Mask pattern, a) Source/drain, b) Gate, c) Contact, d) Metallization, e) Passivation layer, f) Bonding pad.

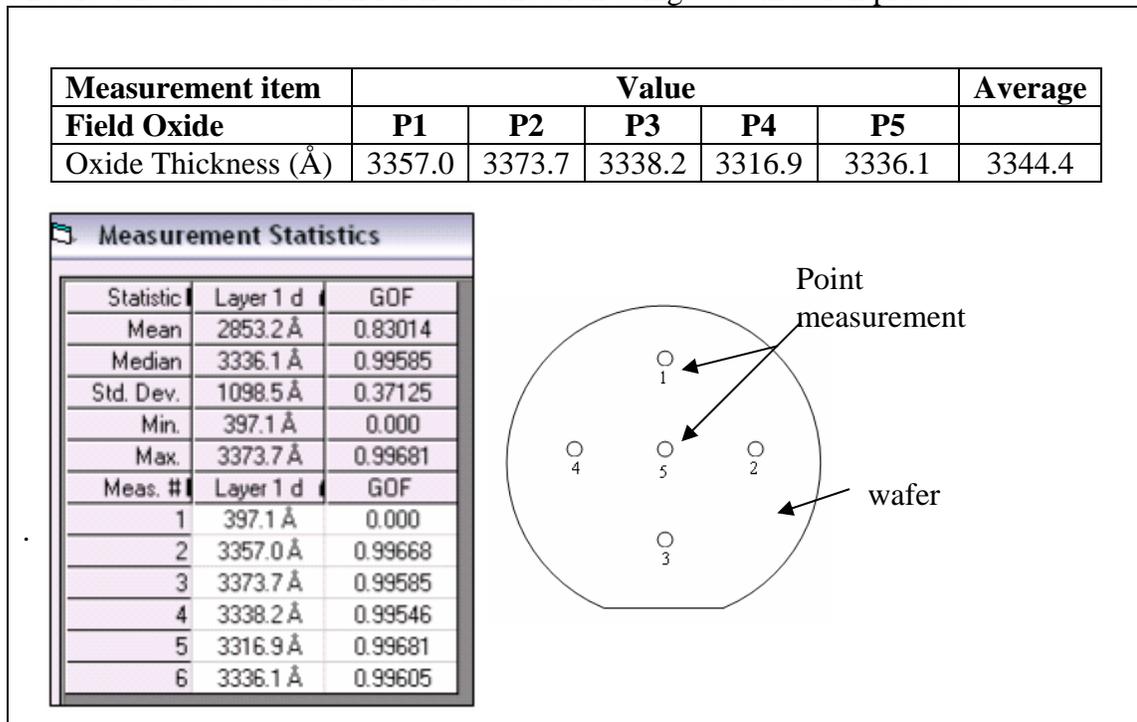
4.1.2 Field oxidation using wet oxidation method

Firstly, the substrates had grown oxide in a high temperature (1000 °C) furnace that cause the Si and O₂ to react and became SiO₂ on the wafer surface. The reaction can be expressed as:



After the oxidation process had completed the process followed by measured the oxide thickness using spectrophotometer. To get the accurate thickness five different points are taken on surface wafer. The thickness of the oxide layer is about 3344.4 Å as show in **Table 4.1**. Purpose growth SiO₂ layer because it can be used as the diffusion mask because their diffusion rate in silicon dioxide is much lower than that in silicon. It reacts with oxygen very quickly, and forms silicon dioxide on the silicon surface.

Table 4.1 : Data collection for field oxidation using wet oxidation process.



4.1.3 Source and drain formation

After completed the process of coating photoresist, soft bake, alignment and exposure UV light, development, etch oxide and strip photoresist, the next stage is visual inspection using high power microscope. The visual inspection is show in **Figure 4.2**. The development process removes the unwanted photoresist and forms the desired pattern defined by the mask 1. The exposed portions are dissolved in the developer solution went positive photoresist is used and developer solution is sensitivity to the temperature. Therefore, both the photoresist and the wafer temperature need to remain constant during this process.

Form **Figure 4.3 a)** show the formation pattern after developer process. Time developer completed remove photoresist and form the pattern is 5 sec. at room temperature. Higher temperature can cause higher chemical reaction rate during the development process, which can induce photoresist overdevelopment and cause critical dimension (CD) loss. Lower temperature can cause lower chemical reaction rate, which can induce photoresist underdevelopment and cause critical (CD) gain or incomplete development. The SiO_2 is etched with buffered oxide etch (BOE) solution is usually used because it attach oxide but not silicon or photoresist. Therefore BOE etches away the oxide in the openings in the photoresist and stops at the silicon surface as show in **Figure 4.3 b)**. After SiO_2 completed etching process about 5 minute, the following next process strip photoresist. Photoresist is stripping by a solvent (Acetone) and the result the pattern is the same as the opaque image on the mask are show in **Figure 4.3 c)**.

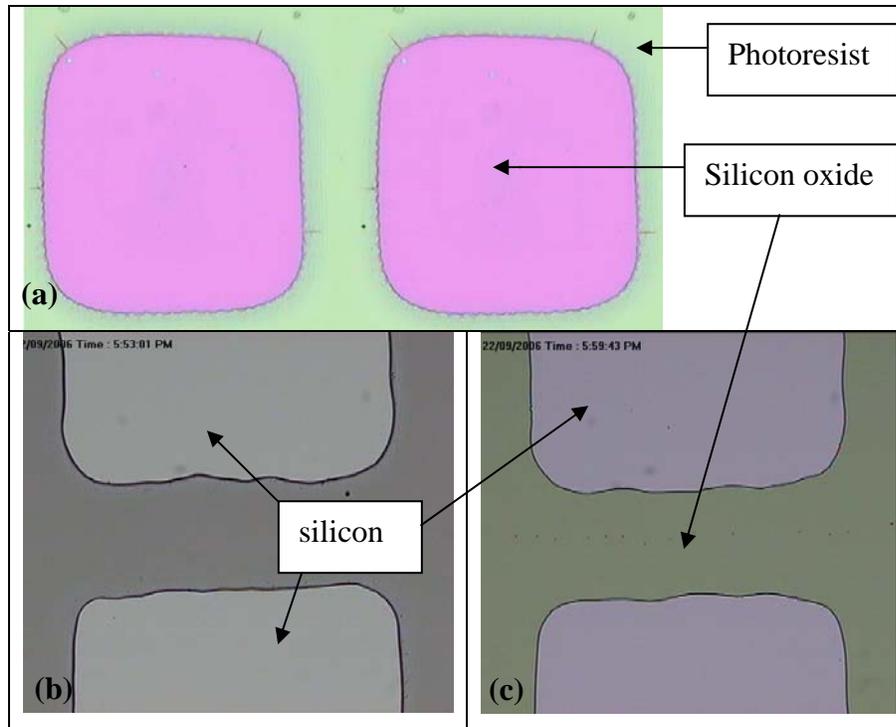
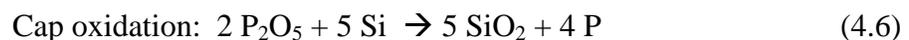
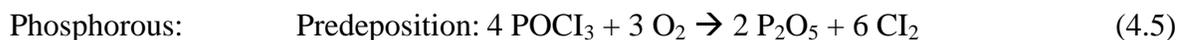
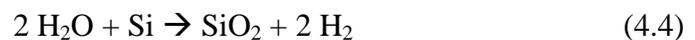
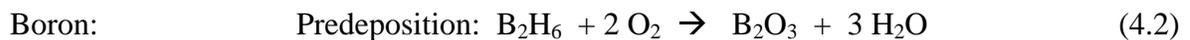


Figure 4.3 Photograph of source and drain formation. a) after develop, b) remove oxide, c) strip photoresist.

After stripping the photoresist, the next process step is formed well where the substrate is not covered with oxide. A two-step diffusion process is used to form drain and source regions, in which (Phosphorus or Boron) predeposition is first formed under a Constant-Surface-Concentration Condition (CSCC) and then is followed by a drive-in diffusion under a Constant-Total-Dopant Condition (CTDC). Finally, a thin layer of (Phosphosilicate or Boronsilicate) Glass on the wafer is removed BOE solution. For a pMOS, the substrate is n-type, and the source/drain are heavily p-type doped such as boron, and for an nMOS, the substrate is p-type, and will deposited phosphorous (n-type) as show in **Figure 4.4**. The chemical reaction of the predeposition and cap oxidation can be expressed as:



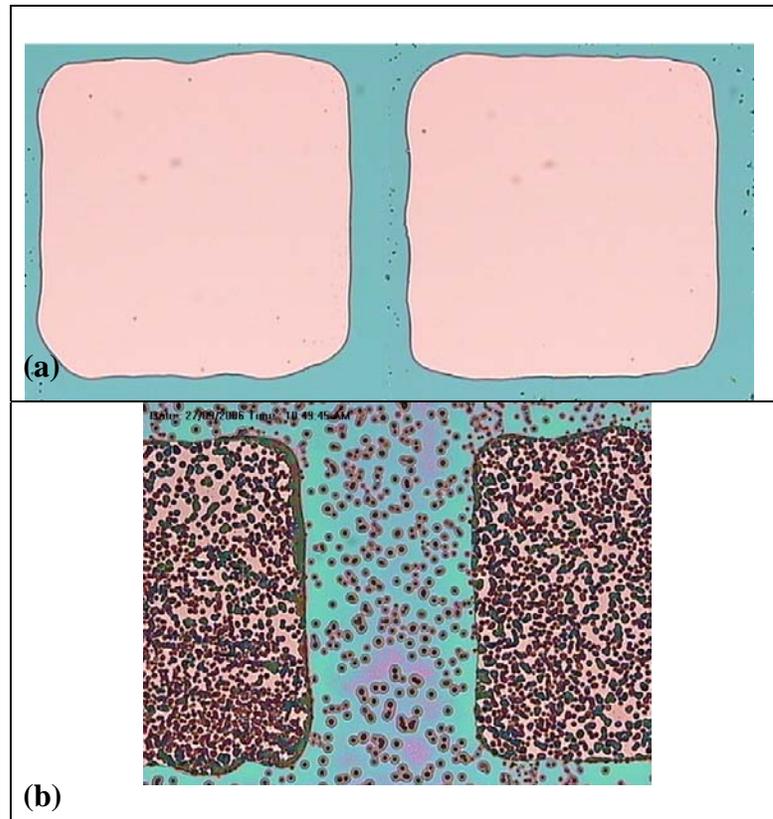


Figure 4.4 Photograph diffusion process. a) dopant with Phosphorous, b) dopant with Boron.

4.1.4 Gate oxide formation

Mask 2 is used for formed gate oxide, and this process is similar with previous process source and drain formation. This process involved photolithography step, including photoresist coating, soft bake, alignment and exposure, development, pattern inspection and hard bake. Time developer completed remove photoresist and form the pattern is 15 second at room temperature, and time remove oxide about 6 minute. The visual inspection for gate formation for pMOS and nMOS as show in **Figure 4.5** and **4.6**.

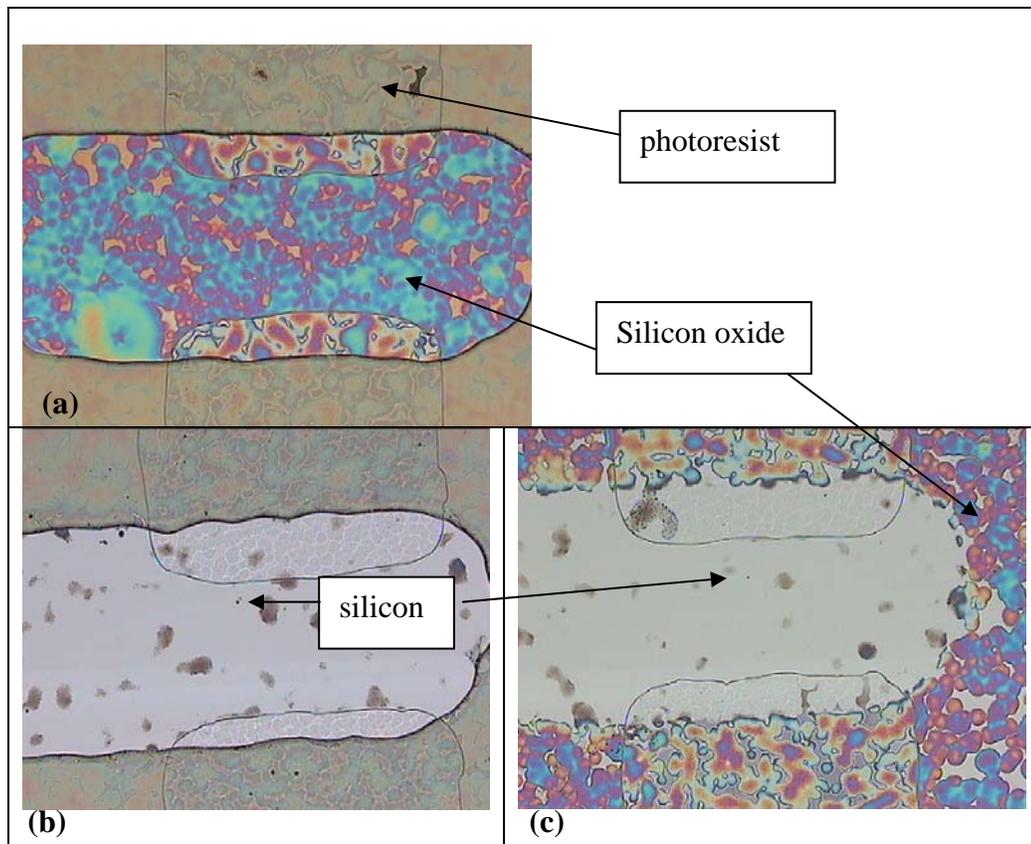


Figure 4.5 Photograph of gate formation for pmos. a) after develop, b) remove oxide, c) strip photoresist.

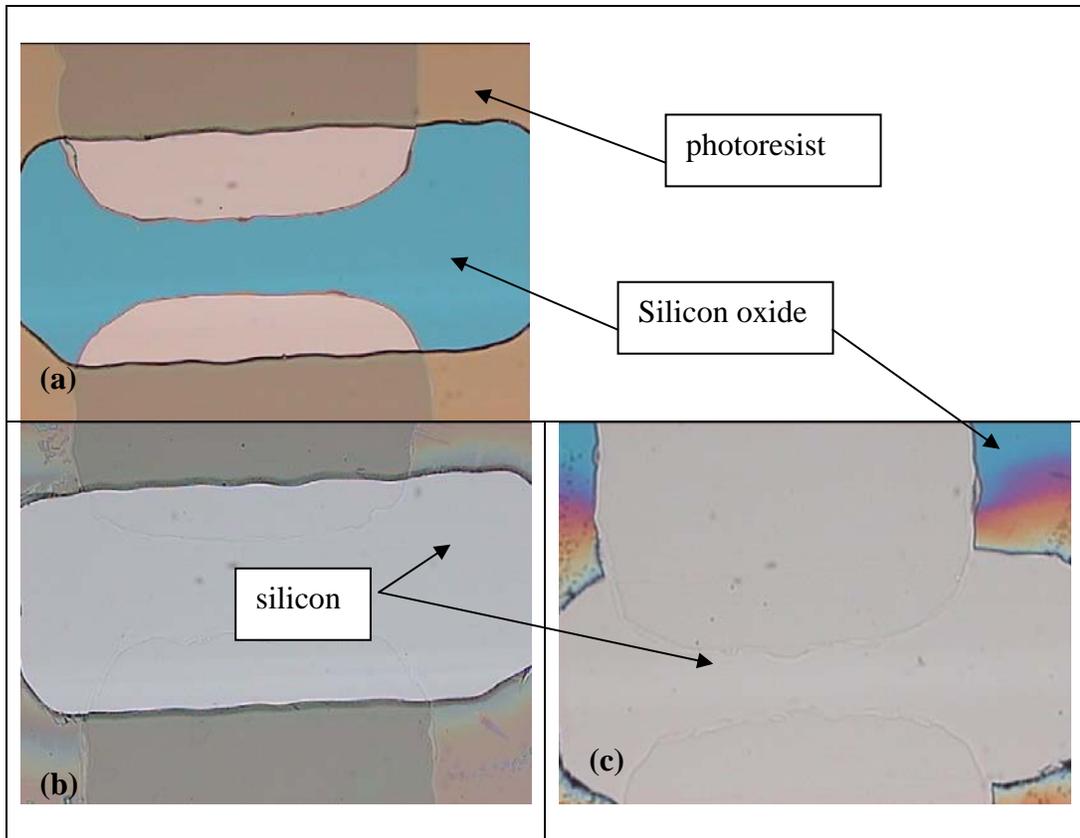


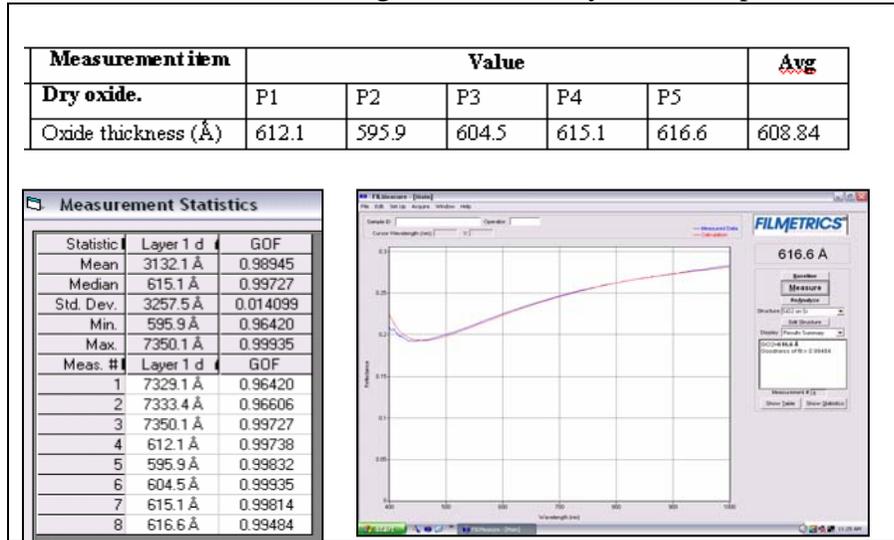
Figure 4.6 Photograph of gate formation for nmos. a) after develop, b) remove oxide, c) strip photoresist

4.1.4.1 Gate oxide using dry oxidation method

After the second photolithography, a very thin gate oxide layer is grown by thermal oxidation. Dry oxidation has a lower growth rate than wet oxidation, but the oxide film quality is better than wet oxide film, therefore dry oxidation are use to growth gate oxide.

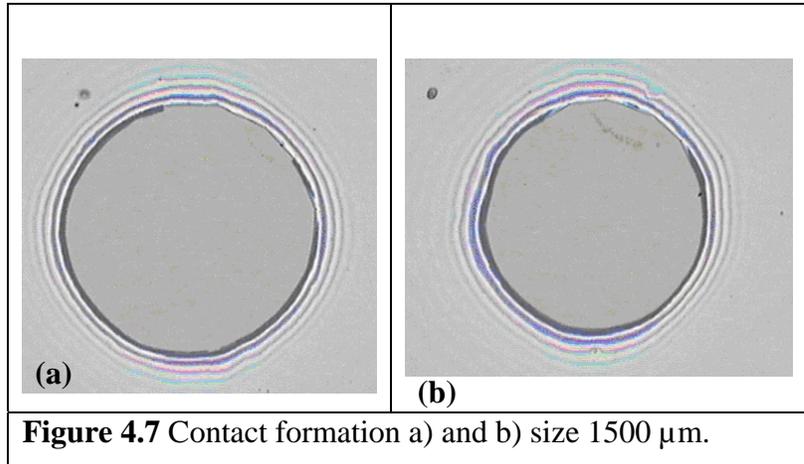
Table 4.2 show the thickness of gate oxide after dry oxidation is about 608.84 \AA .

Table 4.2 Thickness of gate oxide for dry oxidation process.



4.1.5 Contact formation

The next process is pattern contact using mask 3 before deposited aluminium for interconnection and again process photolithography is used for pattern transfer. After coating photoresist, soft bake, alignment and exposed. The problem is after development process, pattern still cannot open window until overdevelop. After that change new developer solution, increase time expose to (110 sec, 150 sec, 200 sec, 250 sec) and review the process photolithography, the result is contact still cannot open window. **Figure 4.7** show the size of contact 1500 μm can open window, the original pattern contact design is square but after development the contact pattern change to became circle. Because of this problem, this project cannot be continuing to the next process and this project is not successful.



4.2 AlNiAu interconnection using lift-off process

AlNiAu as the interconnection involved of several steps. It start with Al deposition, the follow by cleaning, activation and zincation to remove the oxide layer thus, provide good adhesive. The next process is nickel deposition and lastly gold in deposited on top of Ni. Gold is used because of is not easily oxidize upon exposure for environment.

4.2.1 Aluminium bond pad

Figure 4.8 show the analysis on the aluminum bond pad surface morphology using high power microscope, AFM and SEM. In **Figure 4.8 (a)** show the aluminum bond pad and silicon nitride will cover by photoresist layer, elemental analysis using EDX detects Al and Si as bond pad base metal composition as show in **Figure 4.8 (b)**. **Figure 4.8 (c)** shows the roughness aluminum pad using AFM. The thicknesses of aluminum bond pad is not uniformity and not smoothly evaporated during process deposited aluminum and **Figure 4.8 (d)** show the surface aluminum layer using Scanning Electron Microscope (SEM).

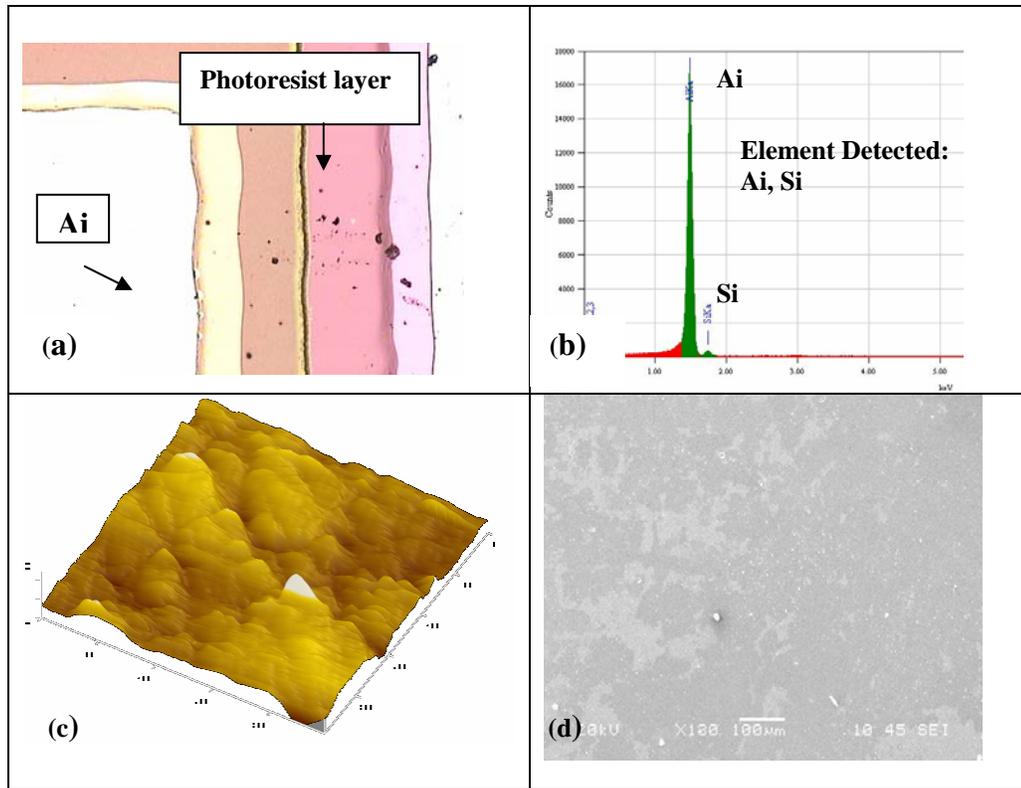


Figure 4.8 : Initial aluminum bond pad surface: a) high power microscope magnification,10x , b) EDX spectrogram, c) AFM microscope image. d) micrograph image (high magnification,100x).

4.2.2 Surface cleaning

Cleaning process is performed to remove various contaminations that were presents on the wafer surfaces that were due to material handling. **Figure 4.9** shows that the surface characteristics and elemental identities of the bond pad were not changed significantly after treatment at this process step, compared to the initial bond pad surface (**Figure. 4.8**).

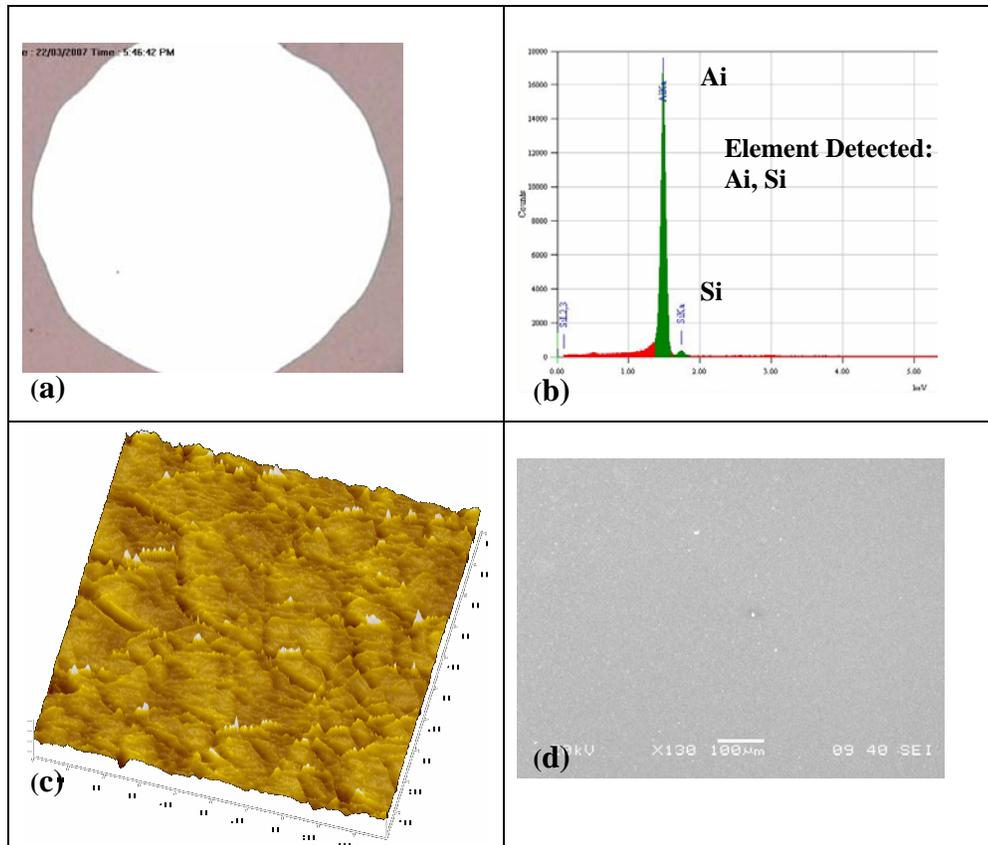


Figure 4.9: After surface cleaning process: a) high power microscope magnification, 10x, b) EDX spectrogram, c) AFM microscope image, d) micrograph image (high magnification, 100x).

4.2.3 Aluminum bond pad activation

The purposes of activation process are to micro-etch the aluminum oxide and activate the surface for better nucleation at subsequent process. **Figure 4.10** show similar results on of surface characteristic and elemental that was detected at this process, compared to previous step (**Figure 4.9**). The activation process resulted clear grain structure on the aluminum surfaces if compared to bond pad at cleaning and initial surfaces as shown in **Figure 4.10(d)**, **4.10(d)** and **4.8 (d)**.

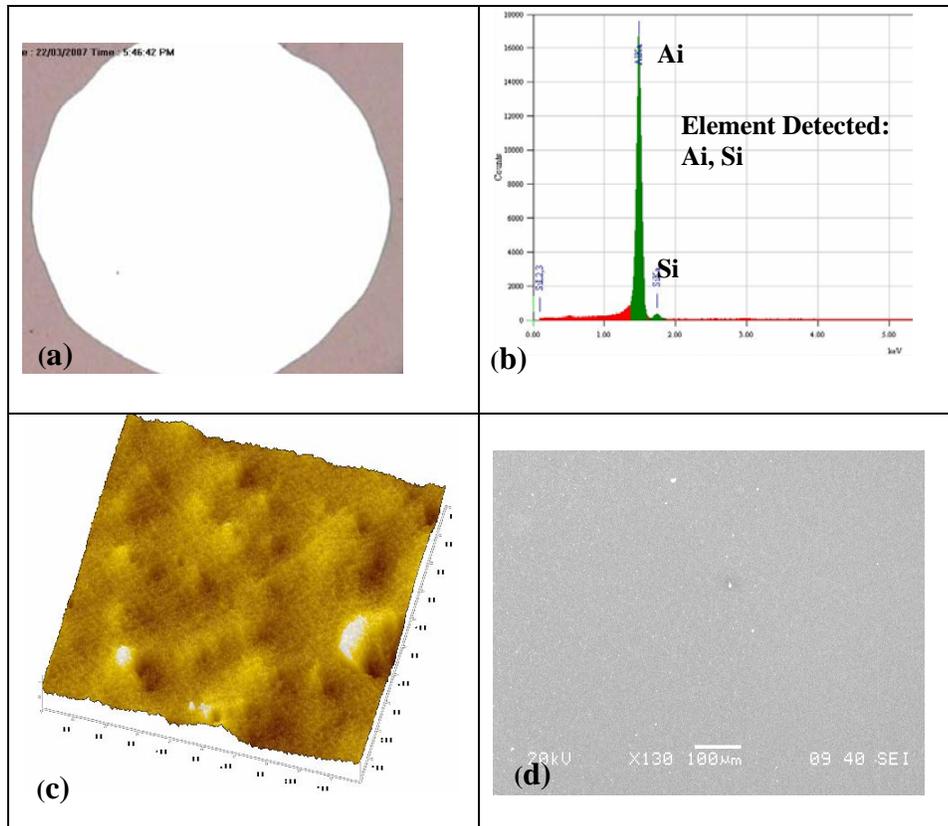
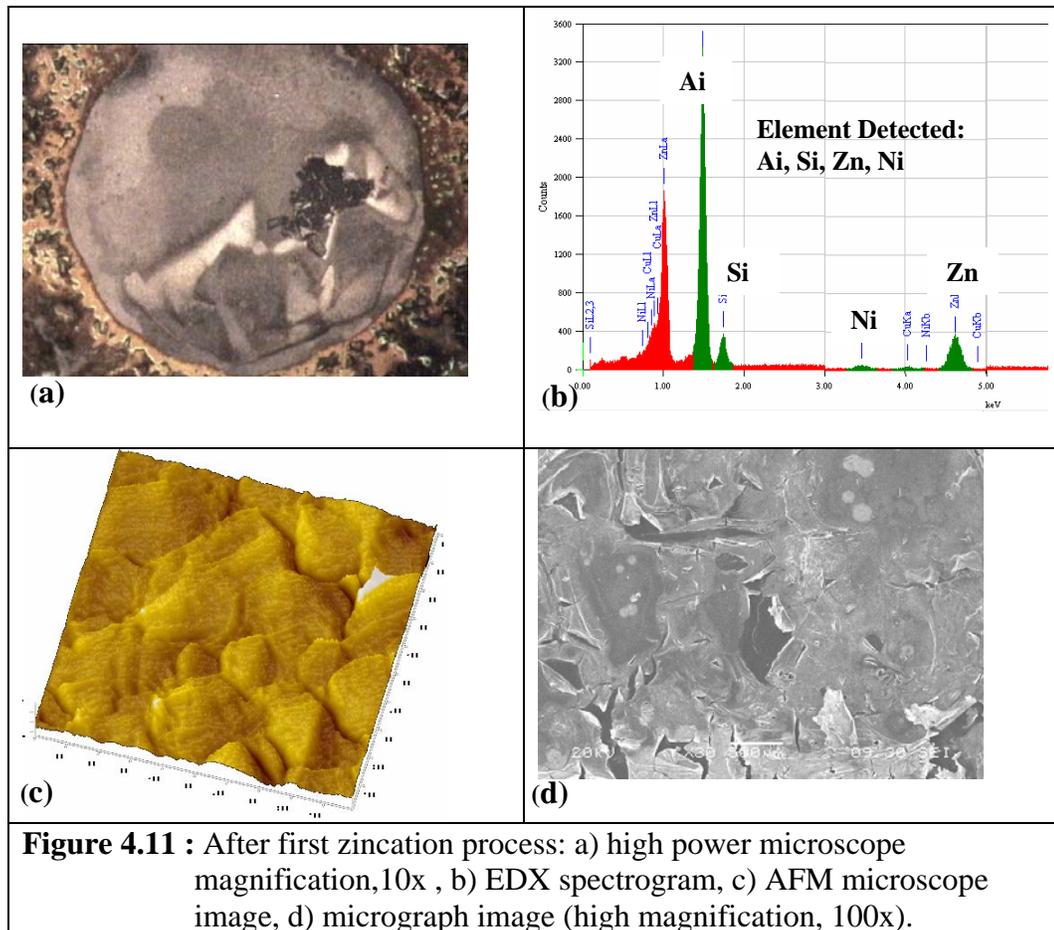


Figure 4.10 : After aluminum activation process: a) high power microscope magnification,10x , b) AFM microscope image, c) EDX spectrogram, d) micrograph image (high magnification, 100x).

4.2.4 First zincation

The zincation is a process of coating the aluminum bond pad with a layer of zinc. The zinc layer will prevent the re-oxidation on aluminum bond pad and to initiate the electroless nickel deposition [23]. During the zincation process the aluminum oxide completely dissolved into solution while depositing zinc on the surface. At this process step, elemental analysis in **Figure 4.11 (b)** show the presence of Zn, Ni, Al, and Si. The first zincation process was not able to eliminate nodules as shown in **Figure 4.11**. Surface morphology of zinc preserved the contour of initial bond pads with present of nodules of zinc on the surface. Also, due to deposition of zinc the bond pad surface getting rougher than previous process and **Figure 4.12** show the effect of using photoresist as a top layer

after first zincation process. Two sample with different top layer (photoresist and silicon nitride) will be immersion into zincation solution. As shows in **Figure 4.12 a)** photoresist layer can prevent from react or damage during zincation process and thickness of photoresist is $2\mu\text{m}$, but in **Figure 4.10 b) and c)** show the passivation layer was damage and react with zincation solution. This is because of thickness silicon nitride is very thin about 5000\AA , and cannot prevent the layer during zincation process.



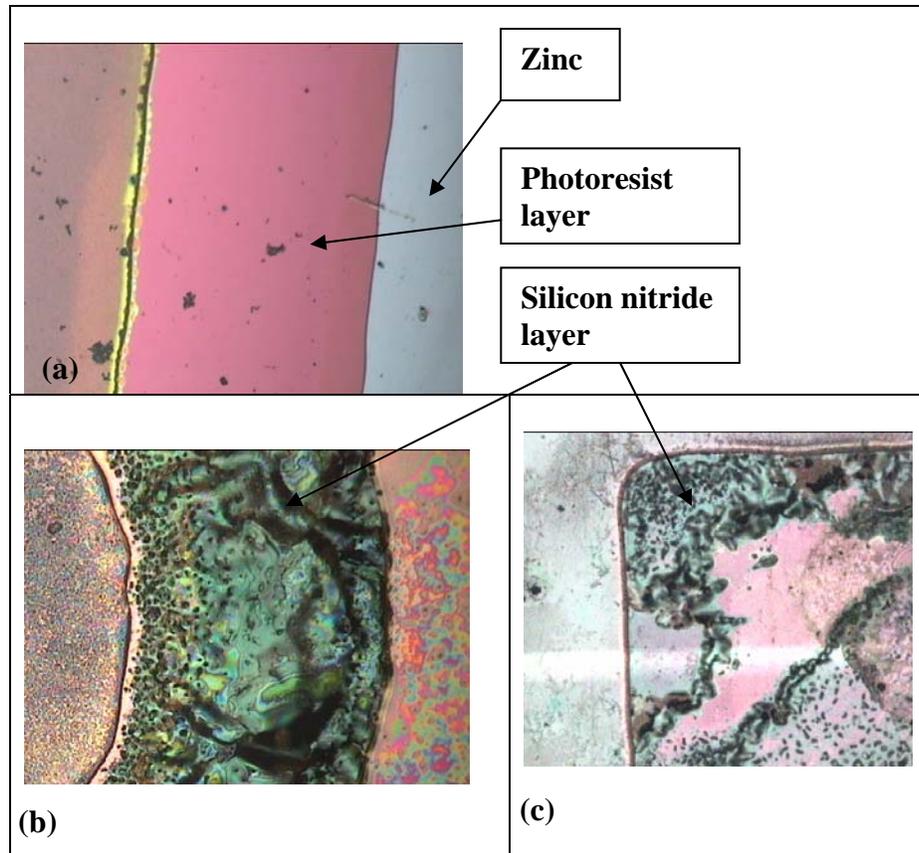


Figure 4.12 : Effect of using photoresist as a top layer. a) using photoresist, b) and c) without photoresist layer.

4.2.5 Zinc removal

At this process the first zinc and nickel layer was removed using the selective etching of nitric acid. Generally nitric acid attacks all the base metals except aluminum, therefore makes it suitable for removing zinc and nickel on the aluminum bond pad surface. EDX analysis proves no other elements detected except the bond pad material composition itself. AFM microscope and micrograph image in **Figure 4.13** shows the surface characteristics back to the initial bond pad surface. However the surface is getting smoother compared to previous process (**Figure 4.10**) because the aluminum surface was etched during the reduction and oxidation at zincation process while depositing zinc and nickel.

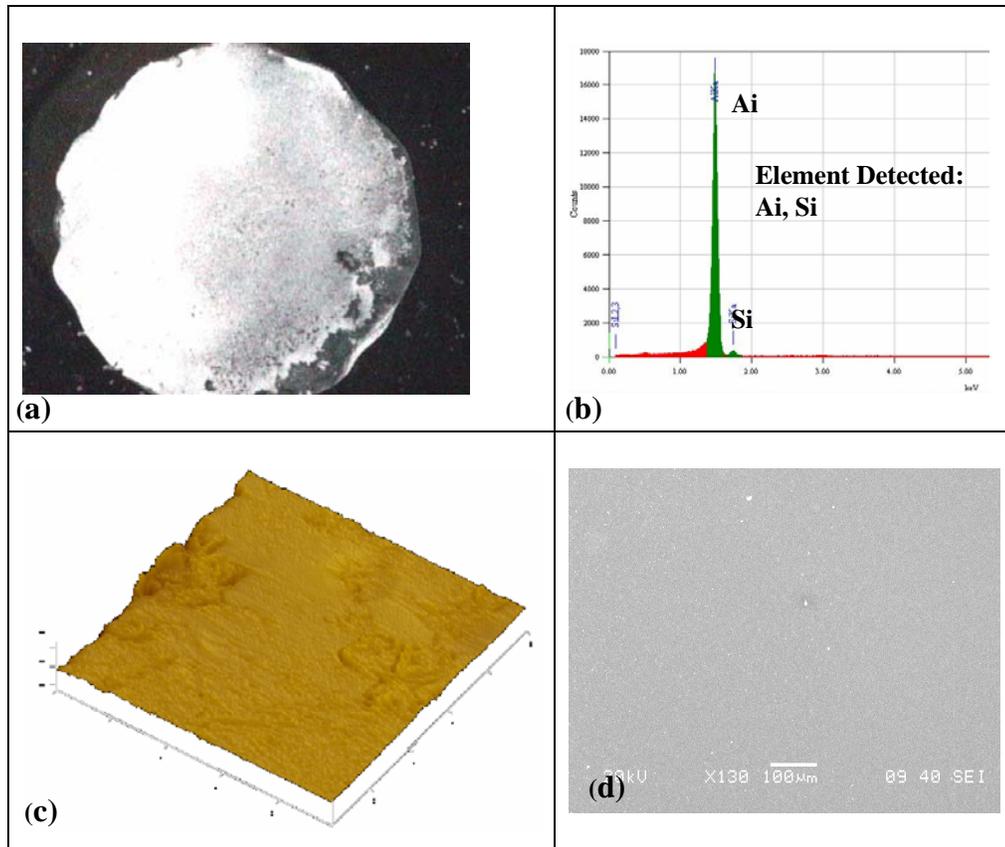


Figure 4.13 : After zinc removal process: a) high power microscope magnification,10x , b) EDX spectrogram, c) AFM microscope image, d) micrograph image (high magnification, 100x).

4.2.6 Second zincation

At this process step, the elemental analysis and surface morphology are similar with first zincation **Figure 4.11**, however it improved the surface roughness as shown in **Figure 4.14**. Double zincation is a common preferred method for plating aluminum and is especially useful on certain difficult-to-plate alloys to ensure better adhesion of the final metal layer deposit. The properties of the metal plate are directly related to the thickness, uniformity and continuity of the zincates coating with thinner coating generally providing smoother and more adhesive metal plating [24]. This result is due to fact that first zincation process attacks homogeneously on the aluminum pad without specifically attack the

existence of nodules on the surface. However, this reaction will refine the size of nodules and make it getting smaller, thus produce better surface after second zincation.

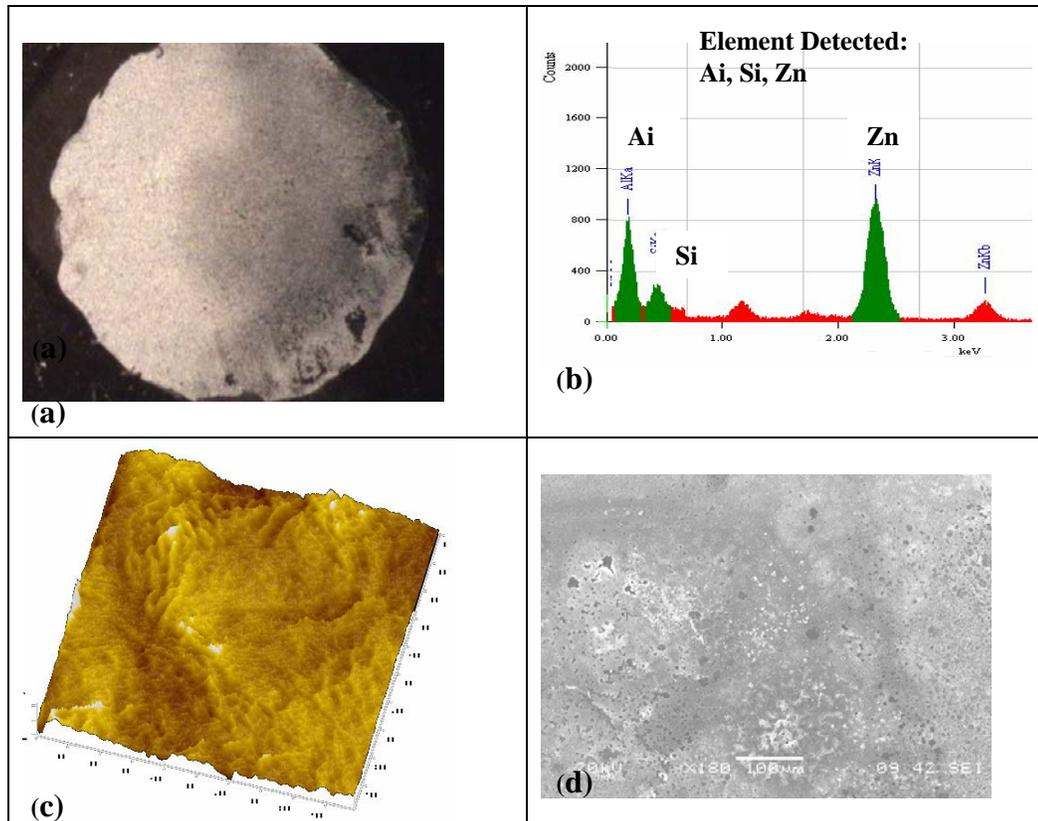


Figure 4.14 : After second zincation process: a) high power microscope magnification,10x , b) EDX spectrogram, c) AFM microscope image, d) micrograph image (high magnification, 100x).

4.2.7 Electroless nickel

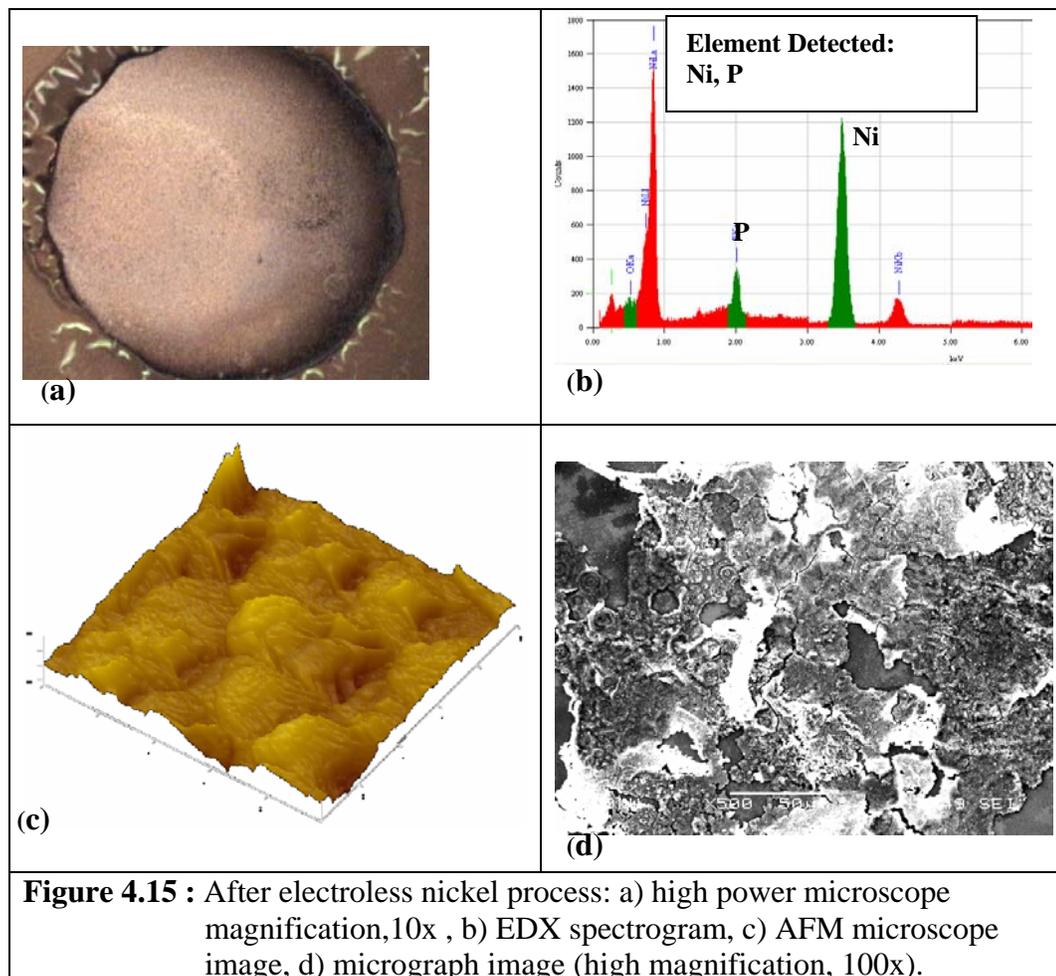
The elemental, microstructure and morphology analysis in **Figure 4.15** shows the surface morphology of zinc was replaced by nickel morphology. Zinc that was used to initiate the reaction was dissolved in the electroless nickel solution during the reaction with ion zinc as following equation:



General formulation of electroless Ni (P) deposition.



Figure 4.15 b) shows that the elemental analysis using EDX detects nickel-phosphorous, (NiP) elements. Phosphorous peak is observed due to fact that the reducing agents in solution used contained hypophosphite.



4.2.8 Immersion gold

An immersion reaction is an oxidation/reduction system in which an ion in solution is reduced to the metal at the expense of the surface metal, which is oxidized to an ion. The exchange occurs in one direction only. This is determined by the relative positions of the interacting metals in the electromotive force series (any metal higher in the electromotive series will displace from solution any metal below it in the series). In immersion plating of gold over nickel, gold ions from solution are reduced to gold metal. The electrons needed for this reduction are supplied by the nickel substrate itself. Immersion deposition or displacement plating will cease as soon as the substrate is completely covered by the immersion coating.

When electroless nickel deposition was completed, the deposition of gold layer was carried out to prevent the surface from oxidation and improves solderability. The gold layer coating mechanism involves exchange reaction occurring between gold ion and nickel known as an immersion process. An immersion process referred to as displacement or replacement processes, depends on the oxidation of the less noble metal surface to supply electrons for the reduction of the more noble metal from solution. In the case of electroless nickel/immersion gold, Au ions in the solution took electrons from Ni atoms because of their difference in galvanic potential. Basically, the overall reaction displacement between Ni and Au in the process is presented as below:



The final process is strip photoresist layer using acetone solution as show in **Figure 4.16 a)**. During process first zincation, zinc removal, second zincation, electroless nickel and immersion gold, the photoresist layer still can prevent the passivation layer. Elemental analysis using EDX detects Au (55.69%), Al (6.79%), and Ni(37.40%) as bond pad base

metal composition show in **Figure 4.16 c**).The presence of Ni (P) from the electroless nickel process and Au element from immersion gold process as shown in **Figure 4.16**. Using AFM surface morphology Au layer can determine show in **Figure 4.16 d**) the surface not deposited uniformly and smoothly. The micrograph images were taken using Scanning Electron Microscope (SEM) at 200x magnification as shown in **Figure 4.16 e**).

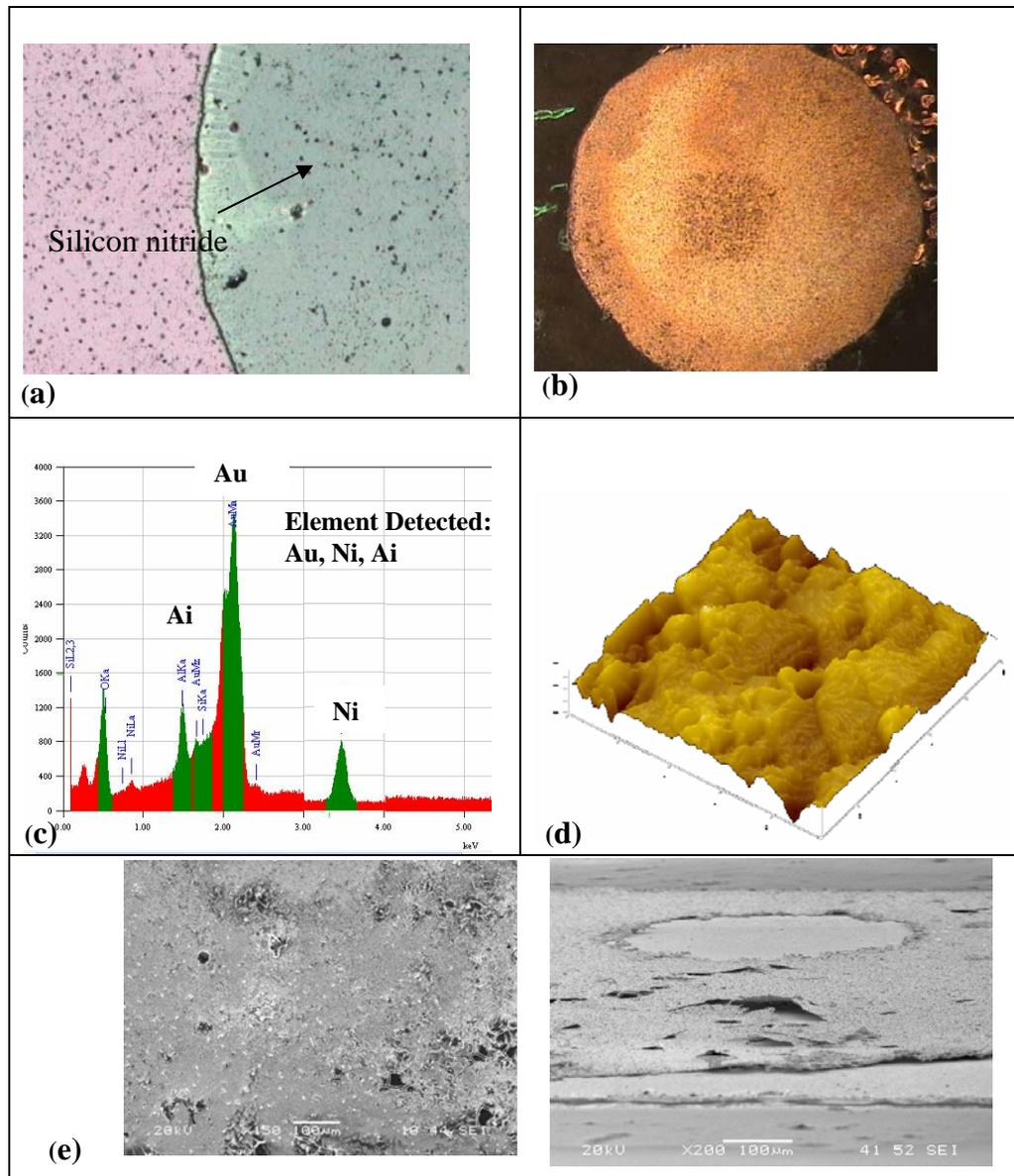


Figure 4.16 : After immersion gold process: a) Strip photoresist layer, b) high power microscope magnification,10x , c) EDX spectrogram, d) AFM microscope image, e) micrograph image (high magnification, 100x).