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ORIGINAL ARTICLES

Fabrication of Polysilicon Nanowires using Trimming Technique

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ABSTRACT

Recently most researches are more to scaling down the electronic devices and this fact including component, structure and complexity of electronic devices. These matters also include fabrication of nanowires in certain electronic device which use this application. Nanowires at the present time widely used in many applications such as biotechnology or biosensors, photonics, diodes and field effect transistors (FET), solar cells and so on because it suitable with devices that involve with nanometer scale features, measure and detection or sensors. Nanowires mostly used in biotechnology because the natural size scales of biology itself. This review is to explore more about nanowires and summarizing the important things that related with Nanowires such as structure sizes, fabrication technique will be used and applications involve will be elaborated as well.

Key words: scaling down, electronic devices, nanowires, biotechnology, nanometer scale features, natural size, fabrication technique.

Introduction

Research on CMOS nanostructures such as nanotubes, nanowires and nanobelts hasbecome the focus intensive for fellow researcher because of their unique properties and can be fabricated with a wide range of materials whether inorganic or organic electrical conductors, semiconductors and insulators (Adam K *et al*, 2006 and Ampere A Tseng, 2008). Besides that without CMOS technology, many devices will not exist as it is now and facing many problems.In this review, there are many problems involves such as difficulty on off-current suppression, difficulty on increase in on-current, difficulty on decrease in gate capacitance, production and development cost increase as mention in now day (Hideyuki Kamimura, 2009). Nanostructure is a structure that assembles from thick or thin layer on silicon wafer until become nanometer scale structures by control the certain process involves. Nanostructure technology makes every manufacture product faster, lighter, stronger, smarter, safer and cleaner. In order to form a nanometer scale structures, two methods need to approaches in nanostructure such as nanowires which is are top-down and bottom-up approaches. Top-down approaches as origin mentioned by Richard Feynmann back in 1950s, larger machines are used to produce a smaller ones and the small ones will be useful to build a tiny machines and so on (Ampere A Tseng, 2008, R. H. J. Hannink and A. J. Hill, 2006). Modern microlithography or nanolithography using a different top-down approach based or depend on technique such as photolithography and other additive and subtractive processing. The top-down method start with a larger structure and with patterning and etching or machining small features with different nanostructure are created. Normally, the top-down method always involve in etching process whether wet or dry etching but both process should always pay more attention because to avoid any unsuspected etching profile. Trimming process is a process that usingInductively Coupled Plasma Reactive Ion Etching**,** ICP-RIE (dry etch)to form a nanostructure. The reason ICP-RIE should be use because ICP-RIE is controllable, high etch rate and high anisotropic profile which is good in producing nanowires structure. Meanwhile, in the bottom-up approach, the atoms and molecules are assembled one at a time in a predetermined order. Bottom-up approaching provides components that made of singles atom or molecules, which are held together by covalent bonds that are far stronger than the forces in microscalestructures (R. H. J. Hannink and A. J. Hill, 2006). Among the bottom-up approaches used to grow nanowires and most of processes are based on vapor liquid solid (VLS) mechanism (Wu, Y.; Yang and P. J. Am. Chem, 2001) using chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD) (Novotny and Yu, 2009), molecular beam epitaxy (MBE) (Jabeen F., Rubini S. and MartelliF., 2009), or laser-assisted catalytic growth (GudiksenM. S. *et al*., 2001) and Figure 1 show those two approaches.

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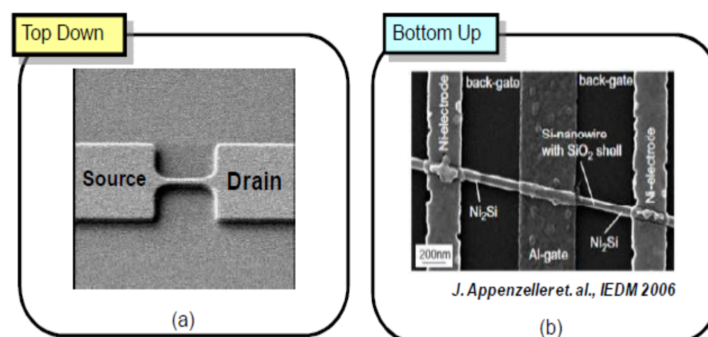

Fig. 1: Fabrication methods of Si nanowire FET,(a)Top-down,(b)Bottom-up [3].

There are several type of nanostructure will be review below and with technology evolve from time to time, nanotechnology has make remarkable enhanced materials will enable a weight reduction accompanied by an increase a stability and an improved functionally.Firstly, nanowires is a structure that has been fabricated with diameter of the order of a nanometer (10^{-9} meters and 1nanometer is corresponds to thousandth of a single strand of human hair) but typically nanowires have diameters of 10-100 nm or less and lengths of 100nm to tens of microns (Ampere A Tseng, 2008). Nanowire structures has many materials can be used such as silicon, polysilicon, silicon nitride and so on. There are five different types of nanowires: Metal nanowires, Semiconductor nanowires (such as Silicon nanowires), Oxide nanowires, Multi-segment nanowires, Semiconductor quantum wires.In order to create molecular nanowires, the process involves repeating organic or inorganic molecular units in a particular ways and the advantage of the nanowire to electronic device are the high quality with nearly perfect surface, nanowire is a scalable nanostructure with precisely controlled critical dimension, it has a high transport low dimensionality structures and it also can be used as both and interconnect for circuit or logic.Nanowires are promising materials for many novel applications because not only for their unique geometry, but also because they possess many unique physical properties including: electrical, magnetic, optical, and mechanical properties. Mostly nanowires are used asinterconnects for nanoelectronics, magnetic devices, biological labels, chemical and biological sensors.

Secondly, other nanostructure that exist is quantum dots which another promising technology for nanoengineering, nanotechnology and microfluidic-based biosensing platform. Quantum dot is a conducting island of a size comparable to the Fermi wavelength in all spatial directions. Often called the artificial atoms, however the size is much bigger (100 nm for quantum dots versus 0.1 nm for atoms). In atoms the attractive forces are exerted by the nucleus, while in quantum dots–by background charges. This is similar by a replacement of nucleus by its neighbor in the periodic table. Quantum dots are main ingredients of modern and future nanoscience and nanotechnology (Chung S *et al*., 2003). The quantum dots' inherent characteristics offer several benefits to microfluidic based detection schemes, such as allowing for increased sensitivity and multiplexed detection. Recently, quantum dots have been used in microchannel assays including antigen-antibody binding for microbe and virus detection (Liu W-T *et al*., 2005Lucas LJ *et al*., 2007,Zhang Q *et al*, 2006).The advantages of using quantum dots in application are the potential to store information to the molecules level and the devices use this applications is sensitive to light and can make a usage of a single electron charges and plus, with ultra-low power consumption, very small size and in theoretically quantum dots only can emit single wavelength of light that similar to gas lasers (Chung S *et al*., 2003). Alivisatos P. *et al*. (Alivisatos P, 2004,Bruchez M *et al*., 1998, Chan WCW *et al*., 1998, Jamieson T *et al*., 2007) mentioned in his studies that quantum dots have provided a great breakthrough in many biological labeling applications with their typical core size of 1–10 nm and outstanding fluorescence compared to typical organic fluorophores. Quantum dots fluorescence comes about as a result of quantum effects from the three-dimensional spatial confinement of the quantum dot's core semiconductor atoms. This confinement limits the core atoms' electron excitation states with the end result being that discrete fluorescence emission is produced with broad excitation. This unique type of fluorescence produces a fluorophore that is bright, photostable, has sharp fluorescence peak, and has colors that are controllable by varying size and composition of the core atoms. These properties have in turn enabled several novel uses of quantum dots in bio-detection methods. Among those uses is multicolor bio-labeling (Chan WCW *et al*., 2002, Ho YP *et al*., 2005, Jaiswal JK *et al*., 2003), achieved by simultaneous use of different quantum dots as well as the use of different quantum dot color and intensity combinations.

Thirdly, another nanostructure that well-known among researcher is a nanogap structure.Nanowgapwidely used in biotechnology as biosensor applications because of ability of nanogap to sense any liquid such as blood or human cell (DNA, protein and so on), chemical solution and even gases. Carbon is a most famous and widely use as nanogap material and a key attribute of high performance nanogap devices is the ability to minimize the tip size and position, and at the same time control the nanoscale gap size precisely (Jun Hyun Han1 *et al*., 2011). There is various methods of conductive nanogap nanofabrication have been developed: mostly direct electron-

beam lithography (M. D. Fischbein and M. Drndic, 2007), mechanical pulling (M. A. Reed *et al*., 1997), shadow masking (E. P. D. Poorterea *et al*., 2006), electromigration(G. Esen and M. S. Fuhrer, 2005), electroplating (L. D. L. S. Valladares *et al*., 2010), focused ion beam (FIB) (T. Nagase *et al*., 2006), angled metal evaporation (S. M. Dirk *et al*., 2005), and silicon micromachining (K. Iwami *et al*., 2006,V. Milanovic *et al*., 2000, M. Mita *et al*., 2005). Most nanogaps are fabricated by laborious serial processes that would introduce a large variation in gap sizes or on a substrate that would interfere with electrical and optical measurements. Figure 2 below is an example that show two images from Jun Hyun Han*et al*. (Jun Hyun Han, 2011) studies and his project.

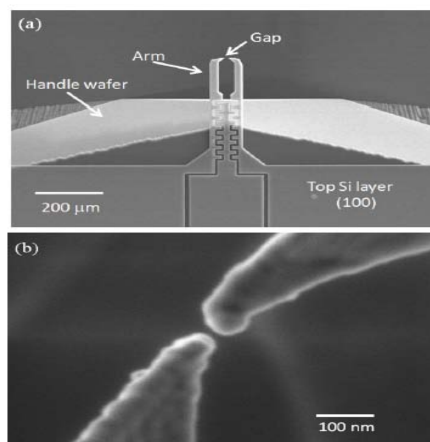

Fig. 2: Free-standing nanogap on an SOI wafer. (a) Overview of nanogap device. The top Si layer is physically and electrically isolated from the handle wafer by buried oxide. (b) Close-up of the ~17 nm gap formed by atomically sharp tips (Jun Hyun Han, 2011).

Lastly, another nanostructure also very popular at the present nanotechnology is nanotubestructure. Same as other structures, nanotube widely used in biotechnology applications but it not impossible to use in other applications such as in nanoelectronic devices, microelectronic devices or chemical. Material usually use in nanotube applications is carbon but still other material also suitable to use like polysilicon, silicon and so on. A nanogap electrode means an electrode having a gap distance of about 1-100 nm (UdaHashim *et al*., 2011). Figure 3 below is an example studies has been done on nanogap.

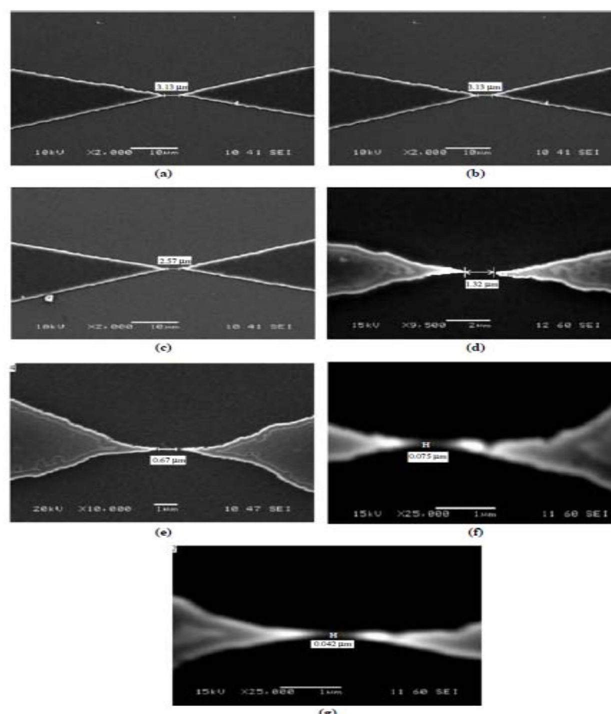

Fig. 3: SEM image of polysilicon pattern after dry oxidation for (a) 1 h (b) 2 h (c) 3 h (d) 4 h (e) 5 h (f) 6 h (g) 7 h (sample 1) (UdaHashim *et al*., 2011).

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Technique:

In this review paper, experimental procedure will explore more detailed about nanowires fabrication and structure. Nanowires are self-assembled pillars grown layer by layer epitaxially. Their positions and dimensions can be controlled with great accuracy (T. Mårtensson *et al*., 2004) and with top-down method Magnus Jonsson *et al*. (Magnus Jonsson, 2005)have fabricated trenches inGallium Phosphide nanowires for integrating with microfluidics. The general method of making masks is to spin coat a photo resist on the sample and produce patterns with UV photolithography to uncover the underlying substrate. In order to seal the trench, authors have deposit with a plain layer of PDMS (polydimethylsiloxane) and therefore start somewhat differently. Previously, Magnus Jonsson *et al*. have proved Silicon Nitride to bond to PDMS after oxygen ashing so a thin permanent bottom layer of Silicon Nitride will be deposited onto the substrate (B. in Figure 4). A photo resist is then spin coated on the sample and the pattern is formed by UV-photolithography (C in Figure 4). The same pattern is later transferred to the underlying layer of Silicon Nitride by reactive ion etching (RIE) and the masking is finished (D. in Figure 4). The pattern in the resist is now to be transferred to the underlying layer of Silicon Nitride by reactive ion etching (RIE), which is an anisotropic dry etching method with certain size (E. in Figure 4). Afterwards, the whole wafer is placed in an etchant solution for wet etching process. The sample reacts with the etchant and Gallium Phosphide (GaP) is chemically removed (F. in Figure 4). Anisotropy gives a better etching profile and an increased maximum aspect ratio.

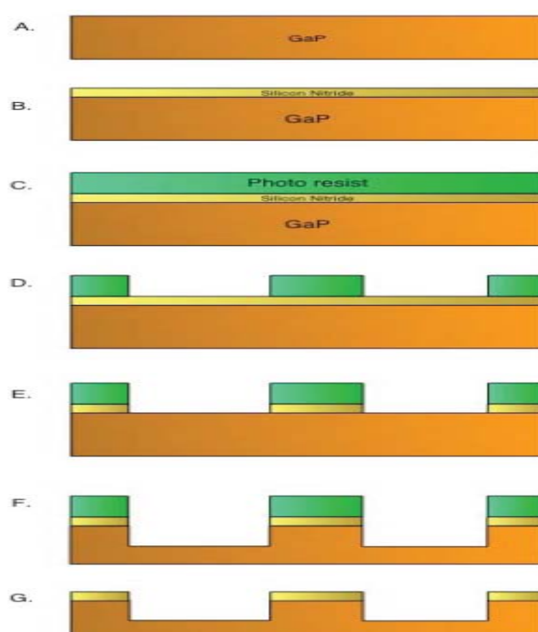

Fig. 4: The procedure of making trenches in GaP. A. Start. B. Deposition of Silicon Nitride. C. Spin coating of photo resist. D. Photolithography. E, RIE on Silicon Nitride. F. Wet etching. G. Removal of existing resist(Magnus Jonsson, 2005).

Another experiment using different material but almost all of a process is a same method. Yugang Sun, Rachel A. Graff, Michael S. Strano, and John A. Rogers*et al*. (Yugang Sun *et al*., 2005) using Gallium Arsenide (GaAs) as wires in their research and Figure 5 below explain a detailed the concept for producing GaAs of structures. First, GaAs wire arrays are prepared by anisotropically etching a GaAs(100) wafer patterned with mask stripes (SiO_2 or photoresist) along the $(0\overline{11})$direction.When the stripes are surrounded by broad features of the mask material, chemical etching produces GaAs wires with ends that connect to the wafer. These connection points pin the GaAs wires at their ends; they hold the wires in the positions defined by the pattern of mask stripes even when the wires are completely undercut. Resist patterns are then defined (in some cases by conventional photolithography) onto the pinned wire arrays (step ii). These resist features serve as masks for modifying the properties of the exposed segments of the wires. Yugang Sun, Rachel A. Graff, Michael S. Strano, and John A. Rogers *et al*. demonstrate here three possibilities: 1) Etching exposed sections of the wires and then removing the resist to produce GaAs wires with alternating widths (step iii), 2) depositing materials (such as metals) onto the exposed sections to form GaAs wires with segments composed of alternating compositions (step iv), and, as described in detail in a following section, 3) anisotropically etching exposed regions to form wires with complex cross-sectional shapes.

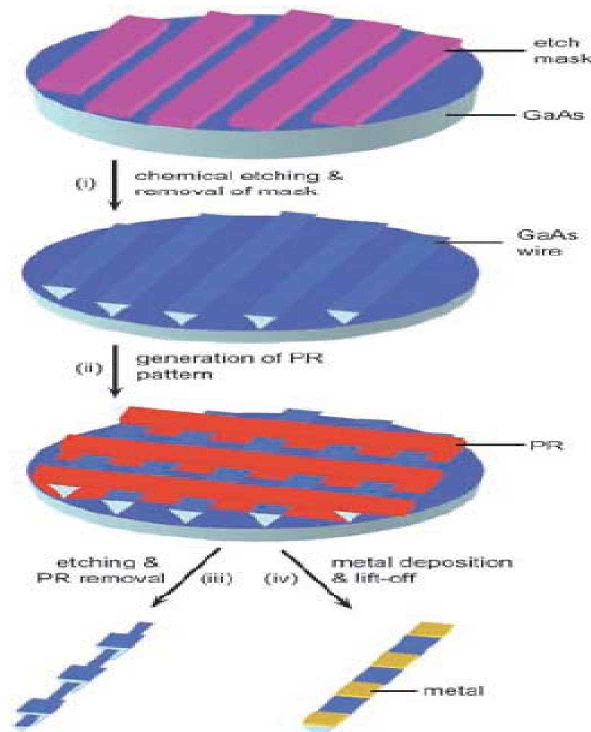

Fig. 5: Schematic diagram for fabricating GaAs wires with alternating dimensions or compositions along their longitudinal axis. The steps include: i) preparing an array of GaAs wires with a triangular cross section from a GaAs(100) wafer patterned with mask stripes along the $(0\overline{11})$direction and anisotropically etched in an aqueous solution consisting of H_3PO_4 (85 wt%), H_2O_2 (30wt %), and H_2O (1:13:12 in volume); ii) patterning the resultant wire array (after removal of the etch mask stripes) with photoresist lines perpendicular to the orientation of the GaAs wires; and iii) etching the GaAs wires using the photoresist as a mask to generate wires with alternating widths, or iv) depositing metals through the photoresist pattern to create GaAs wires with segments alternating in composition (Yugang Sun *et al*., 2005).

Hua Wang, Minghua Sun, Kang Ding, Martin T. Hill, and Cun-ZhengNing *et al*.(Hua Wang *et al*., 2011)fabricated their nanowires using two different material which areIndium Phosphide (InP)and Indium Galium Arsenide Phosphide(InGaAsP) as shows in Figure 6 including result from fabrication and result will be elaborate later. While Fabrication process, two wafer samples was used for nanowire fabrication to demonstrate the powerfulness of the method. The first one is a commercial S-doped n-type InP (100) wafer and the second wafer is a custom-designed epitaxial heterostructure grown by a commercial vendor on an InP (100) substrate. The nanowires were obtained from wafer pieces after etching in a Surface Technology Systems (STS) ICP-RIE system. An etching cycle consisted of one-minute of etching using a gas mixture of methane (CH_4) and hydrogen (H_2), followed by 10 s of O_2 plasma treatment (OPT) carried out in the same ICP-RIE chamber. The cycle was repeated for tens of times in order to get desired length of the nanowires. During the CH_4/H_2 etching, coil power, which is the RF power supply inductively coupled to a coil electrode wrapping around the chamber wall, was set at 125 W, while platen power, which is the other RF power supply inductively coupled to a platen electrode connecting to a sample chuck, was set at 75 W. Both RF power supplies are operated at 13.56 MHz. CH_4 and H_2 were introduced into the chamber at 30 standard cubic centimeters per minute (sccm) and 20 sccm flow rate, respectively. The process pressure during the CH_4/H_2 etching was 15 mTorr. According to our experience of etching patterns defined by hard masks, the above condition gives the etched patterns smooth and vertical sidewalls. While the CH_4/H_2 etching was fixed at the optimal condition, the processparameters of O_2 plasma treatment were varied to study the relation between the O2 plasma treatment and the formation of the nanowires. Unless mentioned otherwise, the O_2 plasma recipe used in this study is as the following: the O_2 flow rate was 49.5 sccm, the process pressure was 40 mTorr, and the coil power and platen power were 1000 and 30 W, respectively.

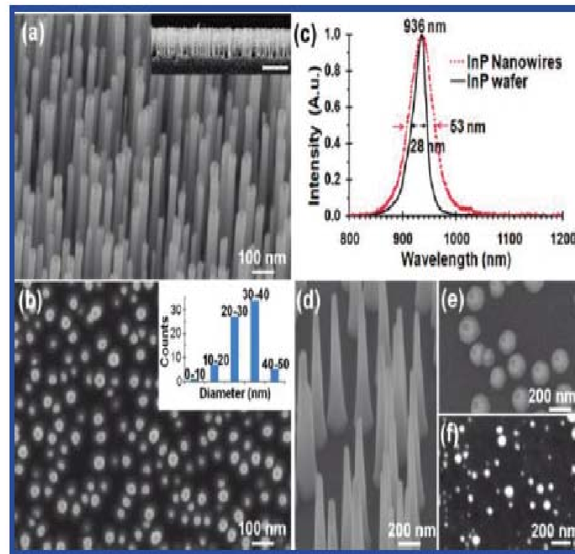

Fig. 6: SEM images and PL spectrum of etched nanowires. (a) Tilted view SEM image of rod-shaped InP nanowires formed with 30Wplaten power for O_2 plasma treatment (OPT); inset shows side view of the nanowire array (scale bar = 1 μm); (b) top view of nanowires shown in (a) with inset showing diameter distribution; (c) room-temperature PL spectra from rod-shaped InP nanowires and wafer; (d) tilted view of cone-shaped nanowires formed with 60 W platen power for OPT; (e) top view of the nanowires shown in (e); (f) top view of the nanowires formed with 40 W platen power for OPT(Hua Wang *et al*., 2011).

Another material (InGaAsP) also not much different but to demonstrate the real potential of this approach, Hua Wang, Minghua Sun, Kang Ding, Martin T. Hill, and Cun-ZhengNing *et al*. (Hua Wang *et al*., 2011)use a similar process to produce wires with much more complex longitudinal structures. The epitaxial heterostructure with 16 custom-designed layers was grown on InP(100) substrate with doping profile across many layers and a middle layer structure of InGaAsP(G)/InGaAs/InGaAsP(G) with composition graded quaternary layers, as shown in Figure 7(a). The corresponding band edge profiles are shown in Figure 7(d). Figure 7(b) and 7(c) shows schematic of nanowires etched from the epitaxial multilayers shown in Figure 7(a).

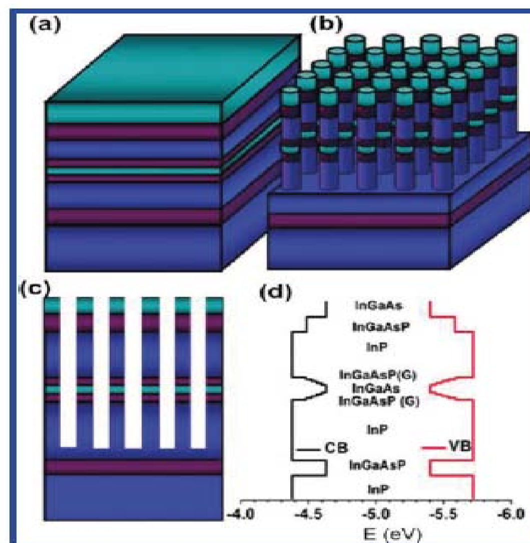

Fig. 7: Schematic of heterostructure wafer and nanowires. (a) Schematic of heterostructure wafer on InP substrate; (b) nanowire array after etching; (c) 2D view of the heterostructure nanowire array; (d) corresponding band-edge profiles of conduction (CB) and valence band (VB) across the layers (along the wire axis direction after etching). The InGaAsP (G) layers represent stepwise composition graded layers with a thickness of 20 nm each with P composition increasing from 13 to 60% starting from InGaAs layer of 20 nm thick to both sides(Hua Wang *et al*., 2011).

Results:

Magnus Jonsson *et al*. (Magnus Jonsson, 2005)successfully deposit the Silicon Nitride layer on the sample in photolithography process. Areas under the holder arm did not get covered of obvious reasons. The layer was around 84nm thick according to previous experiments. A mask with 10µm channels separated by 10µm was used to produce stripes of the positive photoresist (S1813) on the sample. The stripes were not perfectly smooth and there were also many major defects. Many trenches were clogged by resist at the edges due to defects from the spinning process (Figure 8C). However, since Magnus Jonsson *et al*. only had one sample covered with Silicon Nitride and decided to use it and move on to the next step in the process. Magnus Jonsson *et al* have etched for 100s with estimated etching rate of 1.17nm/s which gives a depth of around 117nm. This is thicker than the estimated value of the deposited layer of Silicon Nitride and the surface of the trenches was now Gallium Phosphide again. Optical images show that damaged areas from the photolithography got worse after RIE (Figure 8C-D),however the channels were not as much affected and still acceptable. Unfortunately, the resist clogging the trenches at the edges were not removed by the reactive ion etches.

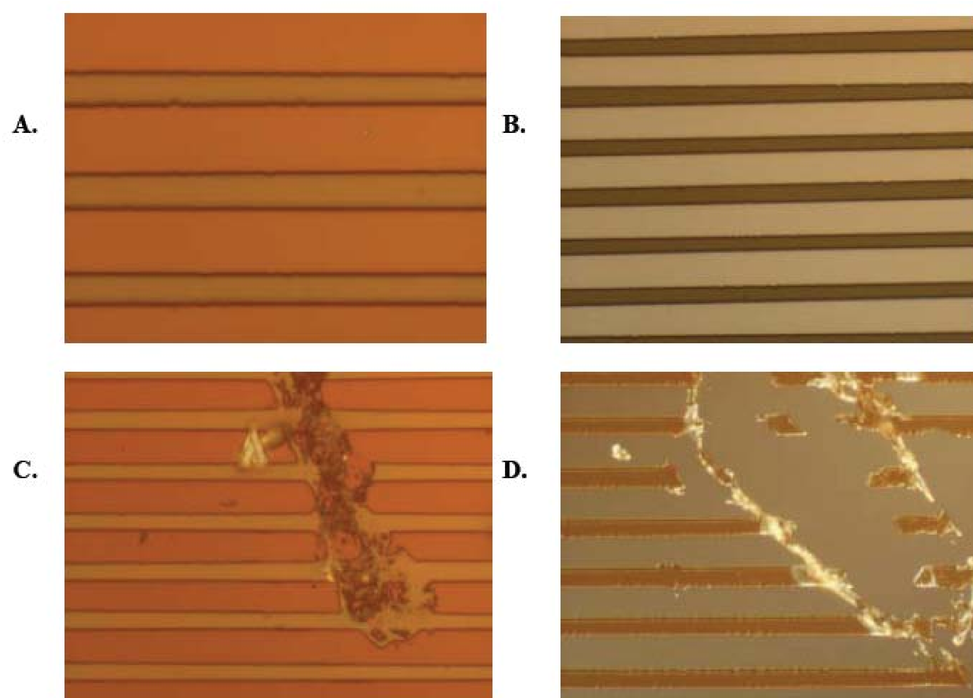

Fig. 8: A.After photolithography. S1813 on GaP covered with SixNy 100X magnification. B.After RIE, 50X. C. Damaged area before RIE. D. same damaged area after RIE(Magnus Jonsson, 2005).

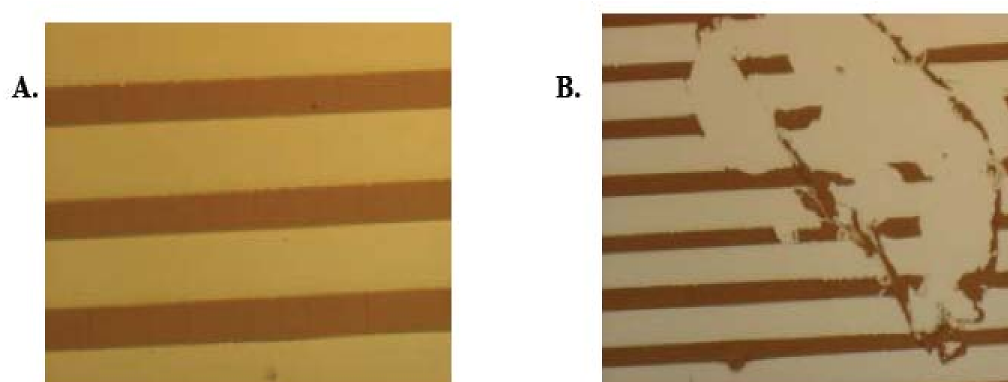

Fig. 9: A. Trenches in GaP after wet etching, 100X. B. Same damaged area as in Figure 8C-D (Magnus Jonsson, 2005).

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After wet etching in 20 min, a channel in the GaP wafer was made and the result did not differ much from the previous pattern in the resist (Figure 9A-B). The wet etch did not further increase the damaged areas (Figure 9B), which implies that Silicon Nitride and S1813 was a good choice as etching mask. The etching depth was around 200nm which gives an etching rate of 10nm/min.

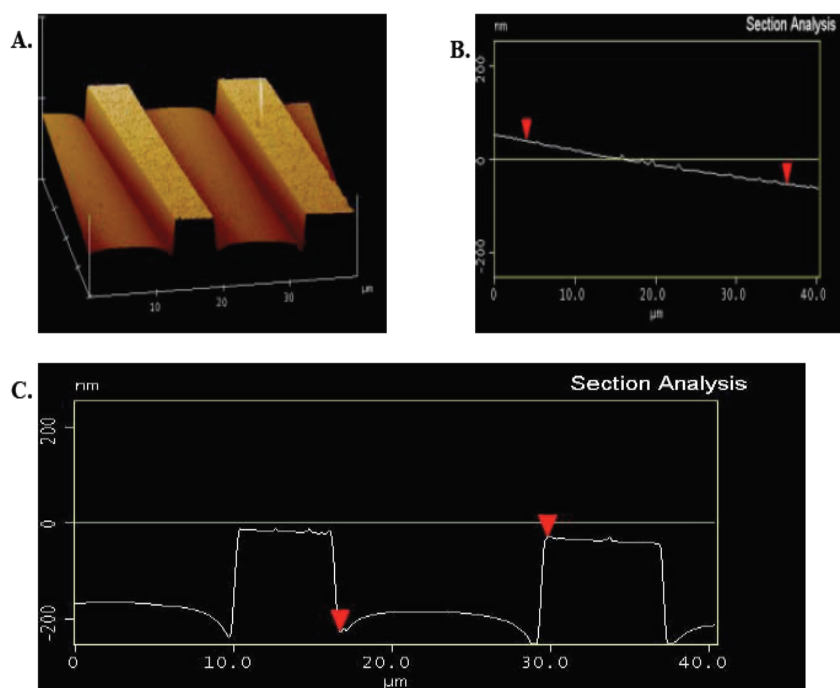

Fig. 10: A. 3D image of the trenches in GaP after wet etching. B. Surface roughness along one trench. C. Profile of the trenches. These images were made with a Nanoscope 3100 Dimension AFM (Magnus Jonsson, 2005).

The profile is shown in Figure 10B. The surface roughness along one trench is shown in Figure 10B and the surface is flat with a variation of few nanometers, which must be considered to be very smooth (observe that x and y axis have different scales). After cleaning the sample it was delivered for deposition of Gold particles and subsequent growth of nanowires(Magnus Jonsson, 2005).For Yugang Sun, Rachel A. Graff, Michael S. Strano, and John A. Rogers *et al*. (Yugang Sun *et al*., 2005) experiments', samples will undergo SEM for taking images as result. Figure 11 shows scanning electron microscopy (SEM) images of GaAs wires before and after selective etching for different durations. Figure 11A shows an SEM image of an array of wires on awafer as obtained by etching (H_3PO_4 (85 wt%):H_2O_2 (30 wt%):H_2O=1:13:12 in volume) through masks of parallel SiO_2 lines (with a width of≈2 mm). Wires produced in this fashion have widths (W) of ≈400 nm; they retain the alignment established by the photolithography. The anisotropic etching continues even if the wires lift off from thewafer. As a result, the widths of the GaAs wires can be decreased down to 50 nm by controlling the etching time. To produce more complex structures, the wafer is spin cast with a photoresist film that can be patterned into lines perpendicular to the orientation of GaAs wires, that is, along the $(0\bar{1}1)$direction.The inset gives an SEM image of a broken wire, clearly showing its triangular cross section. The height (H) of this wire (i.e., the perpendicular distance between the sharp ridge released from the wafer and (100) top surface) is ≈650 nm. As shown in Figure 11C, the sections of the wires not coated with photoresist were etched anisotropically, with some undercut. The widths of these open sections were reduced, indicating that the side walls of each wire were also etched. Figure 11D shows a random assembly of several broken wires with their side walls facing the SEM detector. Unlike the uniform etching over the exposed (100) top surface, anisotropic etching of the side walls removes a layer of GaAs with a V-shaped profile. The sample is shown in Figure 11B, is soaked in etchant, etching initiates from the (100) top surface because this surface is more chemically active than the side surfaces. Because both edges have a higher probability of being etched than the middle part of the top surface of each wire, the vertical etching rate alongside walls is higher than that of middle part. As a result, a thin layer of GaAs is peeled off from each side wall. Longer etching times continue to shrink the segments exposed to the etchant, thereby increasing the ratio between thicknesses of two adjacent sections of each wire. Figure 11E and 11F show SEM images of a sample obtained by etching the GaAs wires shown in Figure 11B for 45s, illustrating that the width of thinner sections (as indicated by the arrow) is ≈120 nm. The ratio between the widths of the thick and thin

segments is ≈3.4 nm. Different lengths and spacings of these alternating width structures can be achieved easily by the use of appropriate photomasks.

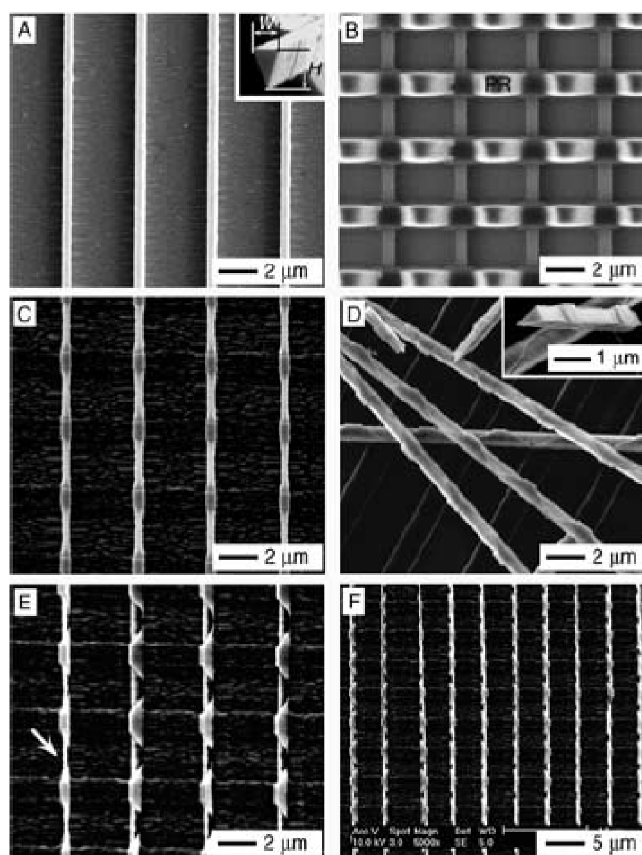

Fig. 11: SEM images of samples obtained by etching 400 nm GaAs wires through ≈1.8 -μm-wide photoresist (PR) lines oriented perpendicular to the wire orientation: A) Parallel GaAs wires with widths of ≈ 400 nm on the wafer; B) a GaAs wire array covered with patterned photoresist lines oriented perpendicular to the wires; C) top-view and D) side-view SEM images of GaAs wires after etching the sample shown in (B) for 20s ; E, F) SEM images of wire arrays after etching the sample shown in (B) for 45 s(Yugang Sun *et al*., 2005).

Hua Wang, Minghua Sun, Kang Ding, Martin T. Hill, and Cun-ZhengNing *et al.* (Hua Wang *et al*., 2011)discussing the resultshown in Figure 6 that the rod-shapedInP nanowires were etched for 20 cycles in total. As can been seen, the individual nanowires were uniform in cross-section along nanowires length. Central area of the round top ends was covered by some material showing dark contrast. The inset of Figure 6a shows the side view of the InP nanowire's, which were relatively uniform in length, with an average length of ∼1 μm. Meanwhile, in Figure 6b shown that the top view of the SEM image and all the nanowires appeared as bright round dots, implying an excellent vertical orientation of the nanowires, which is a unique advantage of the dry etching fabrication method and the diameter of nanowires range is from 10 to 50 nm and mainly centralized from 20 to 40 nm.Figure 6c shows the room temperature PL spectra of InP nanowires and the PL peaks agree perfectly at 936 nm, while the full width at half-maximum (FWHM) of the PL was 53 nm (75 meV) and 28 nm (40 meV) for the nanowires and the wafer, respectively. Hua Wang, Minghua Sun, Kang Ding, Martin T. Hill, and Cun-ZhengNing *et al.* explaining that even without additional treatment, the peak width of etched nanowires was much smaller than that of other InP nanowires grown using bottom-up approaches at around 119, 90 and 84 meV indicating that nanowires have much less surface state effects than those produced by bottom up approaches(BhuniaS. *et al*., 2003, Chuang L. C. *et al*., 2008, Mattila M. *et al*., 2006). As shown in Figure 6d and 6e, the nanowires had a cone shape, and the diameters of the bottom and the top ends of the nanowires were around 150 nm and tens of nanometers, respectively. Meanwhile, result from material InGaAsP also explained base on Figure 12 below. The multilayer nanowires shown in Figure 12(a) were etched for 30 cycles, and the lengths of the nanowires were around 1 μm. Diameter range of the etched multilayer nanowires almost identical with the etched InP nanowires.

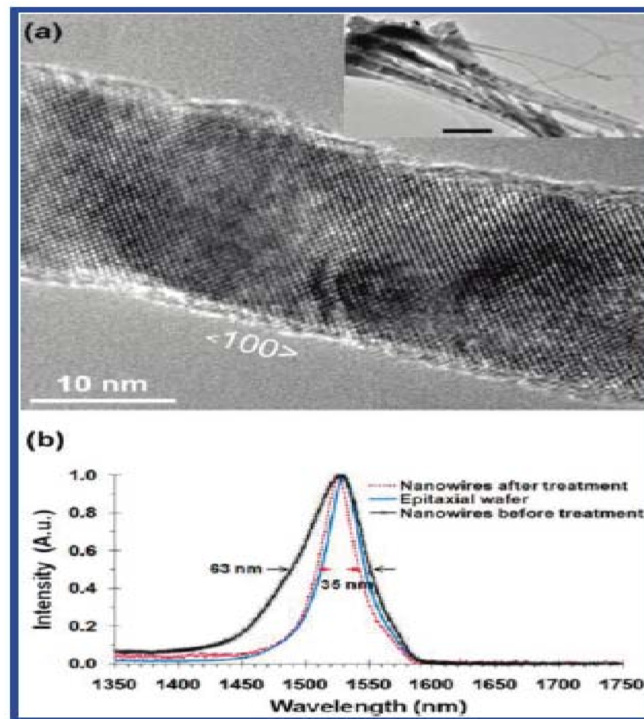

Fig. 12: TEM images and PL spectra of heterostructure nanowires.(a) High-resolution electron microscopy of a nanowire; inset is a lowmagnification TEM micrograph of nanowires dispersed on Cu grid (scale bar = 200 nm). The lengths of the nanowires were around 1 μm; (b) PL spectra at 77 K from the heterostructure wafer (solid line), heterostructure nanowires before (solid line with cross markers) and after (dashed line) chemical treatment (Hua Wang *et al*., 2011).

The increase of PL width of nanowires compared to that of the wafer was caused by the surface damages, as indicated by the 1 nm amorphous surface layer as shown in Figure 12(a). Chemical treatment was performed to remove the surface damages. After it, PL spectrum was measured and shown in Figure 12(b) in dashed line. The FWHM of nanowire after such treatments is improved to around 35 nm (19 meV), which is almost indistinguishable from that of the wafer. Even with a protecting GaAs shell, the linewidth was 87 meV at 14 K for InGaAs/GaAs core-shell nanowires and much wider without the shell.

Conclusion:

Basically, producing a nanowire actually must go through almost same process from the beginning until get a completed fabricate sample for the top-down approach. In other word, some samples almost achieve their target but their samples got some damages while undergo some process such as lithography or etching process as shown in result and discussion section but some other samples got achieved expected result by fellow researcher. All of the experimental has been conducted can be apply in this project because their method similar (using top-down approach) and use all those result as comparison in future and believe this project can contribute in future technology same as others project.

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