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A particle swarm optimization approach for routing in VLSI

Abstract

The performance of very large scale integration (VLSI) circuits is depends on the interconnected routing in the circuits. In VLSI routing, wire sizing, buffer sizing, and buffer insertion are techniques to improve power dissipation, area usage, noise, crosstalk, and time delay. Without considering buffer insertion, the shortest path in routing is assumed having the minimum delay and better performance. However, the interconnect delay can be further improved if buffers are inserted at proper locations along the routing path. Hence, this paper proposes a heuristic technique to simultaneously find the optimal routing path and buffer location for minimal interconnect delay in VLSI based on particle swarm optimization (PSO). PSO is a robust stochastic optimization technique based on the movement and information sharing of swarms. In this study, location of doglegs is employed to model the particles that represent the routing solutions in VLSI. The proposed approach has a good potential in VLSI routing and can be further extended in future.

Keywords — Buffer insertion, interconnect, particle swarm optimization, routing.