A STUDY OF PROPER INTEGRATED CIRCUIT (IC) LAYOUT TECHNIQUES FOR A PARALLEL ADDER

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A STUDY OF PROPER INTEGRATED CIRCUIT (IC) LAYOUT TECHNIQUES FOR A PARALLEL ADDER

by

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APPROVAL AND DECLARATION SHEET

This project report titled A Study of Proper Integrated Circuit (IC) Layout Techniques for a Parallel Adder was prepared and submitted by Kau Zee Shuang (Matrix Number: 071030264) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Microelectronic Engineering) in University Malaysia Perlis (UniMAP).

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KAJIAN TENTANG TEKNIK-TEKNIK BENTANGAN LITAR BERSEPADU YANG BETUL UNTUK SUATU PENAMBAH SELARI

Abstrak

Laporan ini membentangkan teknik-teknik bentangan litar bersepadu yang betul untuk penambah selari. Bentangan untuk penambah selari ini dikemukakan dalam laporan ini. Dalam usaha untuk merancang dan mendapatkan bentangan yang baik, pemahaman mengenai aturan bentangan dan teknik-teknik yang betul diperlukan. Bentangan adalah direka bentuk dengan menggunakan aturan dari teknologi CMOS TSMC 0.35µm. Apabila mereka bentuk bentangan penambah selari, kaedah bentangan seperti ciri-ciri minima, jarak minima, keliling, saiz yang tepat, aturan telaga, aturan transistor, aturan sentuhan dan teknik tertentu seperti susunan pelan lantai, perletakan dan saling hubungan mesti dipatuhi. Penambah selari direka dengan merujuk kepada penambah penuh. Empat individu penambah sel penuh disambung untuk memberi input selari dan membawa riak. Skema dan bentangan penambah selari direka bentuk dalam stesen DA dan IC Mentor Graphics. Bentangan direka bentuk dengan menggunakan Poly, Metal1 dan Metal2 untuk sambungan. Selepas itu bentangan penambah selari selesai dihasilkan, langkah seterusnya adalah simulasi DRC dan LVS. Simulasi DRC dan LVS digunakan untuk mengenalpasti kesilapan yang telah dihadapi oleh pereka. Projek dengan tajuk kajian tentang teknik-teknik bentangan litar bersepadu yang betul untuk suatu penambah selari telah berjaya dihasilkan.

A STUDY OF PROPER INTEGRATED CIRCUIT (IC) LAYOUT TECHNIQUES FOR A PARALLEL ADDER

ABSTRACT

This report presents the proper Integrated Circuit (IC) layout techniques for a parallel adder. The layout produced for this parallel adder is presented in this report. In order to design and to get a good layout, understanding on proper layout design rules and techniques are needed. The layout is designed using rules from TSMC 0.35μm CMOS technology. When designing a layout of parallel adder, layout rules such as minimum features, minimum spacing, surround, exact size, well rules, transistors rules and contact rules and specific techniques such as floorplanning, placement and routing must be followed. Parallel adder is designed by referring to the full adder. Four individual full adder cells are connected to give parallel inputs and ripple carry. The schematic and layout of the parallel adder are designed in Mentor Graphics DA and IC station. The layout has been completed design using POLY, Metal1 and Metal2 for connections. After the layout of parallel adder is finished drawn, the next steps are DRC and LVS simulation. DRC and LVS simulation are used to identify the errors which have all been faced by designer. The project with the title of A Study of Proper Integrated Circuit (IC) Layout Techniques for a Parallel Adder had been successfully.

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