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APPROVAL AND DECLARATION SHEET

This project report titled Quadrature Decoder with Position and Speed Sensing was prepared and submitted by Noradliyah Binti Mohd Murad (Matrix Number: 071030173) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in Universiti Malaysia Perlis (UniMAP).

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PENYAHKOD KUADRATUR DENGAN PENDERIAAN KEDUDUKAN DAN KELAJUAN

ABSTRAK

Penyahkod kuadratur digunakan secara langsung dengan pengekod selari atau tokokan untuk mendapatkan maklumat mengenai arah, kedudukan dan kelajuan dari sistem yang berputar. Ia memainkan peranan penting dalam aplikasi kawalan motor. Projek ini direka untuk mengira kedudukan, kelajuan dan pecutan peranti masukan berdasarkan pada spesifikasi rekabentuk yang diberikan dengan menggunakan Verilog HDL. Rekabentuk ini diselaku dan disahkan menggunakan perisian Altera Modelsim 6.4a. Ragam penyahkodan penuh digunakan untuk peleraian lebih jitu dan ukuran lebih tepat. Pendekatan yang digunakan bertujuan untuk meminimakan penggunaan pendaftar dan menyediakan sistem kawalan yang lebih baik. Pendekatan Verilog HDL yang umum juga digunakan dalam rekabentuk untuk memudahkan penyahpepijatan. Setiap modul memiliki fungsi tersendiri. Penyelakuan dijalankan untuk setiap keadaan masukan bagi memastikan setiap ciri rekabentuk berfungsi. Keseluruhan keputusan membuktikan bahawa rekabentuk yang dijalankan telah berjaya dan memenuhi kehendak spesifikasi rekabentuk.

QUADRATURE DECODER WITH POSITION AND SPEED SENSING

ABSTRACT

Quadrature decoder is used for direct interface with linear or incremental encoder to get direction, position and speed information from a rotating system. It plays an important role in motor control applications. This project is designed to calculate an input device position, speed and acceleration based on the design specification given. It is developed using Verilog HDL. The design is simulated and verified using Altera Modelsim 6.4a software. Full decoding mode is used for finer resolution and accurate measurement. The design approaches aimed to minimize the uses of the registers and to provide a better control system. A common architecture of Verilog HDL is built in order to make design easy to debug. Each module designed has its own function. Waveform simulation is done for every possible input condition in order to check the functionality of each design block. The overall result proved that the design is successfully done and has met the design specification.

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LIST OF ABBREVIATIONS

HDL	Hardware Design Language
CAD	Computer Aided Design
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration
FPGA	Field Programmable Gate Array
CPLD	Complex Programmable Gate Array
RPM	Revolutions per Minute
QEI	Quadrature Encoder Interface
XOR	Exclusive OR
ADC	Analog to Digital Converter