

ESD improvement in P-i-N diode through introducing a lighter and deeper anode junction

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Abstract

Continuous and aggressive miniaturization in the electronic gadget size poses a challenge in solving Electrostatic Discharge (ESD) reliability performance. For diode devices, the shrinkage of the size leads to severe electrical field crowding effect which can cause a total device failure under high ESD surge. Therefore, in this paper, we present a better ESD performance characteristic which can be achieved by optimizing the profile of the P⁺ anode junction of P-i-N diode. The characteristics profile can be altered by lowering the dopant concentration and increasing the depth of the P-i-N diode junction. In this work, comprehensive device simulations, followed by simulation result validation at the wafer level were performed. The ESD surge test was performed and results showed that the changes of the P⁺ anode junction profile on the P-i-N power switching diode can achieve the sustainability of 1 kV ESD surge in the Human Body Model (HBM) and more than 400 V ESD surge in the Machine Model (MM).

Keywords: Electrostatic Discharge (ESD), Human Body Model (HBM) and Machine Model (MM), Forward voltage (VF), Reverse leakage current (IR) and Breakdown voltage (VBR).

1. Introduction

The reliability of the microelectronic devices and circuits is a major factor that determines both their manufacturability and application lifetime. Design for reliability should be implemented during technology, device and circuit development to avoid undesirable product development cycles and costly yield loss and field failures. The field failures caused by Electrostatic Discharge (ESD) events occur on various microelectronic devices inclusive high-power switching diode.

Electrostatic discharge (ESD) is defined as the sudden transfer of an electrostatic charge, which occurs when two electrically charged objects of different potential are brought closely in contact, causing an electrical short or dielectric breakdown [1]. The sudden transfer is characterized by a high current in very short period of a few nano-seconds. There are several types of failures related to ESD, i.e. indirect failures, direct failures and latent failures [2]. Indirect failures or soft errors occur when an edge-sensitive device is falsely clocked by an ESD pulse. Often, the soft error can be recovered by electrical reset. On the other hand,

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direct failure result from the physical destruction of all or part of the device and it is irreversible. Moreover, latent failures are time dependent. When this type of failure occurs, a device will absorb power from an ESD pulse without any physical damage, but over time, the latent failure, which in this case is a reliability failure will cause the device to fail prematurely.

Typically, as the feature chip size becomes smaller, coupled with the increasing complexity of semiconductor fabrication technology, resolving ESD-induced reliability issues have become more challenging [3]. Most commonly used ESD models for the reliability estimation are Human Body Model (HBM), Machine Model (MM) and Charge Device Model (CDM) [4].

In P-i-N power switching diode, the ESD performance can be improved by lowering the electrical fields at the edges of the junction [5]. There are several ways to lower the electrical fields at the edges of the junction such as dynamic-floating-gate technique for the CMOS [6]. The dynamic-floating-gate technique, collaborated with the lightly-doped-drain (LDD) structure had been used to reduce the electrical field around the drain region in CMOS technologies. Secondly, the electrical field at junction edges can be lower by inserting a floating metal ring in GaN-based LED [7]. The floating metal is able to reduce the peak electric field intensity in the semiconductor p-n junction via electrostatic charge induction. Thirdly, the electrical field can be reduced by adjusting the overlap length between the special p-well and the source p+ implantation region in LDMOS. This technique allows the electron distributed evenly from source to drain terminal [8]. Other than the modification on the junction of the device itself, the technique of forming a stack up diode for on-chip ESD protection in CMOS can be used to improve the ESD performance [9]. Most of the conventional techniques that used to improve ESD protection require additional photolithography and etching processes to form additional layer. In this paper, the alteration of the P+ anode junction profile is demonstrated to improve ESD performance. With a constant anode junction depth of the P-i-N diode, a study of a circular shape anode junction's dopant concentration is done to reduce the junction capacitance, with the aim to improve HBM and MM as it is anticipated to provide better product performance and reliability, without major deviation in forward voltage (V_F), breakdown voltage (V_{BR}) and leakage current (I_R).

2. Methodology

The research methodology adopted in this work includes the simulation of the P-i-N diode using Technology Computer-Aided Design (TCAD) simulation software, fabrication of the P-i-N diode, characterization of the current-voltage characteristic at the wafer level, and ESD surge test based on HBM and MM models.

a) ESD Failure Background

Initially, the failure analysis of poor ESD performance units was performed. The post ESD test devices were subjected to de-processing and decorative etches on the sample. The damage observed in the silicon is confined to the edges of the junction as shown in Fig 1. These failures are further shown to be caused by poor ESD. During ESD surge testing, the resultant high current caused momentarily local heating where the design of the junction does not allow heat conduction to the surrounding regions equally. A hot spot can form and lead to metal migration and short-circuit of the junction. This metal migration is called metal spike.

The red arrows indicate the metal spike, which is the weak points for the planar diode at the anode junction curvature in Fig. 1.

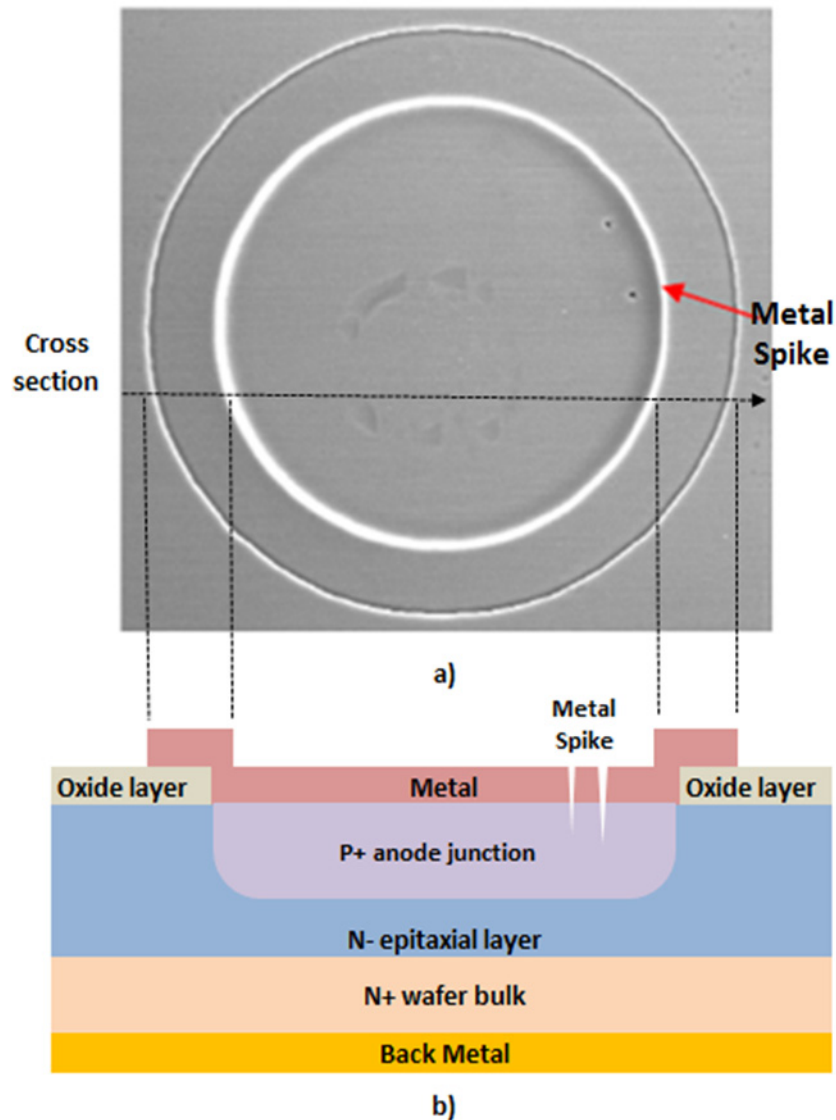


Fig. 1: a) Top view of SEM images of ESD failures diode after de-processing and decorative etches. The metal spike dots that indicated as the red arrow are confined at the edge of junction. b) Cross section illustration of the diode region.

b) Numerical Simulation

Fig. 2 illustrates the cross sectional sketch of the P-i-N power switching diode used in this work, targeting to achieve 300 V reverse breakdown voltage. This P-i-N diode consists of a circular shaped planar boron anode junction diffused into an n-type epitaxial layer over a low resistivity n+ substrate bulk (1.5 - 2.0 m Ω .cm). An n+ diffused isolation region gathers all the defects presence at the perimeter of the anode junction, thus reducing leakage current. The device is simulated considering the technology and design rule development, extraction of compact models and design for manufacturability (DFM) [5]. The simulation splits of anode junction depth and anode junction dopant concentration are defined as the output response of simulation as shown in Table 1. Then, a response surface model (RSM) of a doping profile distribution will be generated by using Tecplot SV interface. In this RSM,

total current density and the impact ionization profile distribution were observed and discussed next in results and discussion section (in Fig. 5 and Fig. 6).

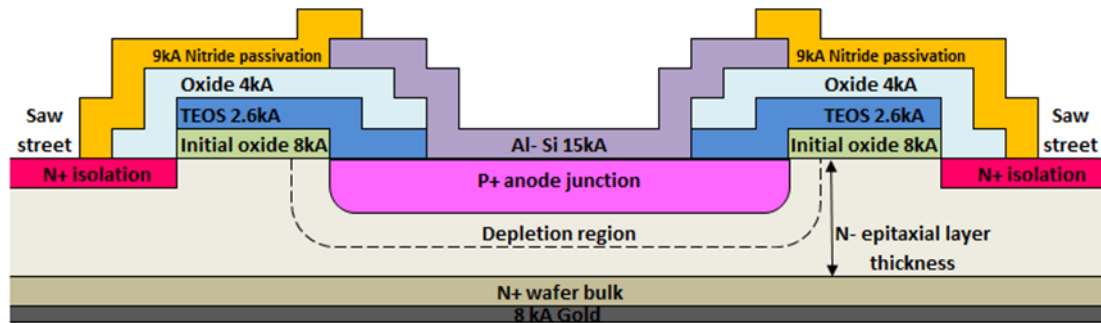


Fig 2: The simulated device cross-section of P-i-N power switching diode

Table 1: Simulation of junction depth and the implant dose concentration of P+ anode junction

Split group	Remark on P+ anode junction profile	Junction depth, μm	Anode junction dopant concentration, ions/cm ²
Control	Control group	1.69	1.0×10^{16}
a	Deeper depth junction	4.69	1.0×10^{16}
b	Deeper depth with lighter doped junction	4.69	5.0×10^{15}

In order to function as power switching diode, the wafer backside is then sputtered with platinum and gold (Au). This is followed by a quick drive-in cycle for both elements, driven through from the bottom of the bulk all the way to the epitaxial layer and the anode junction. The purpose of the platinum is to reduce the reverse recovery time (TRR). While the Au increases, the epitaxial layer resistance which in turn produces a wider P-N junction depletion region to reduce the capacitance.

c) Design of Experiment and Process Split

Based on the result obtained from simulation, a design of experiment (DOE) on the exact wafers material was planned. Fig 3 shows the process flow for the P-i-N power switching diode. The steps as highlighted in yellow (i.e. boron pre-deposition and oxide anneal) are the targeted processes that will be fabricated on the DOE splits. In boron pre-deposition, the parameters of process temperature and time are adjusted to control the anode junction dopant concentration. The oxide annealing is used as the anode junction diffusion process, depending on the temperature and time, translated into junction depth.

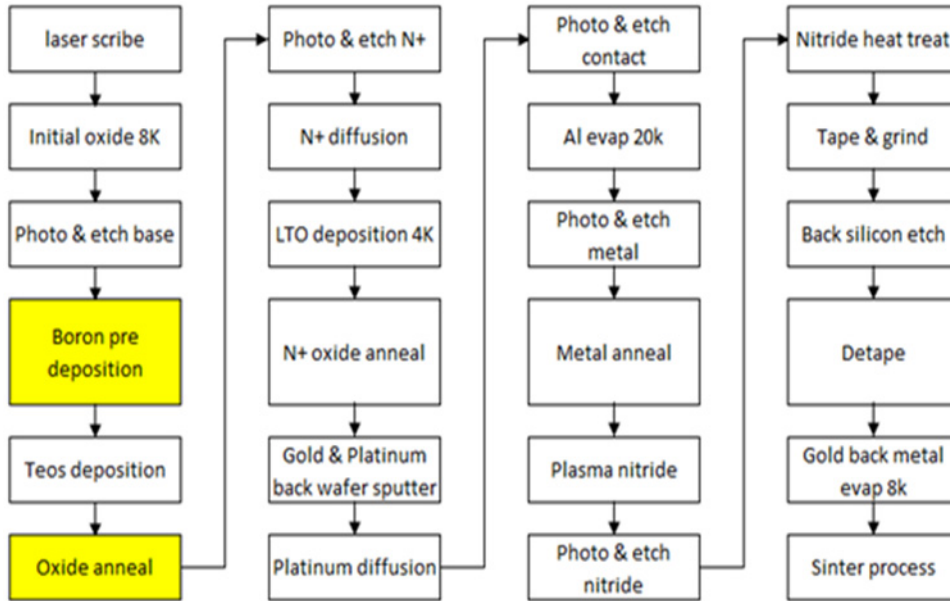


Fig 3: P-i-N power switching diode process flow details

The two variables monitored at anode junction are boron pre-deposition process and oxide anneal. The variation of time and temperature are considered for both processes. Table 2 shows the splits, categorized into four major groups which consist of control group, Group A, B and C. Each group consists of two wafers to ensure the repeatability of the result thus the wafer-to-wafer variation has been taken into consideration.

To create a lighter dopant concentration junction, a lower process temperature is needed during the boron pre-deposition process. A decrease of boron pre-deposition process temperature from 1140 °C to 970 °C based on control group is considered. Low boron pre deposition process temperature is defined in Group B and C. The selection of 970 °C thermal budget is because of the process window on the low side of 15 % less. The difference between low process temperature in Group B and C is due to the process time, which is 15 mins and 23 mins respectively. The purpose of the process time variation is to observe the output respond of V_F and V_{BR} curve.

For deeper junction depth, the process temperature of oxide anneal is increased from 950 °C of the control group to 1200 °C for 25 % increase of the process window. Oxide anneal process time is set at 30 mins.

In Table 2, by adjusting the process temperature and time, the focus is to create a deep junction depth with different levels of lightly doped anode junction.

Table 2: substrate 4 corner split table

Group#	Wafer#	Boron Pre-deposition process		Oxide anneal process	
		Process temperature(°C)	Process time (mins)	Process temperature (°C)	Process time (mins)
Control	1	1140	11	950	30
	4	1140	11	950	30
Group A	3	1140	11	1200	30
	7	1140	11	1200	30
Group B	2	970	15	1200	30
	6	970	15	1200	30
Group C	5	970	23	1200	30
	8	970	23	1200	30

The different anode junction profile creates different curvatures at the anode junction edges. A higher oxide anneals process temperature and longer annealing time will result in a deeper junction depth of planar diode. The lateral diffusion effect will be more significant with a higher process temperature. Hence, a softer curvature of anode junction edge is formed compared to a shallower junction depth of planar diode. The comparison between junction edge curvatures for different junction depth is illustrated in Fig. 4. The curvature profiles are indicated in the red dotted circle. The soft curvature of anode junction edge improves the ESD performance.

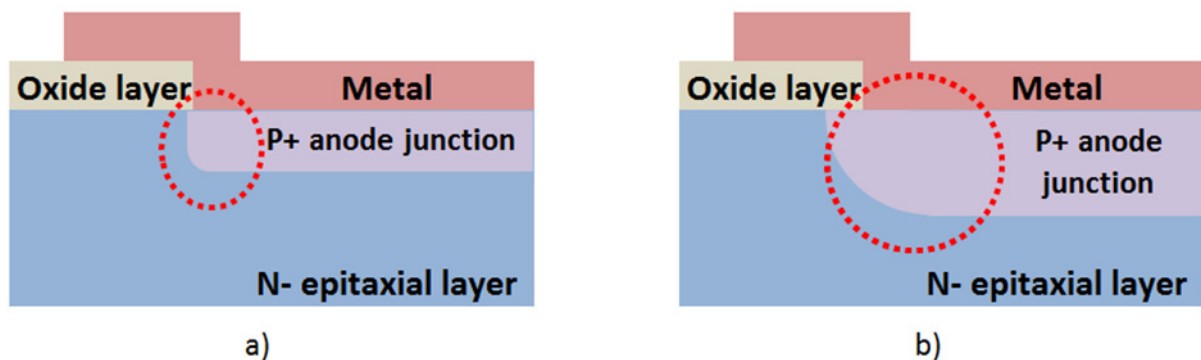


Fig 4: P+ anode junction edges curvature profile for a) shallower junction depth planar diode, b) deeper junction depth planar diodes

The fabricated wafers are then subjected to wafer level electrical testing. Electrical data of V_F , V_{BR} and I_R are collected and analysed using commercial statistical software, i.e. JMP. The study between the control group and evaluation process recipe combination groups are observed. Subsequently, all wafers are sent for assembly and to be subjected to ESD surge test on HBM and MM. The sample size of the ESD surge test is 100 units.

With the electrical and ESD surge test results, a final combination of boron pre deposition process and anode drive in process conditions are determined and validated with qualification lots. A total of 3 qualification lots are processed with the same series of fabrication process flow to test the repeatability in order to anticipate the lot-to-lot variation.

3. Results and Discussion

a) Simulation Result

Fig. 5 shows the total current density doping profile distribution of half diode for three different process combination groups, i.e. control, group A and group B. Based on the simulated result, the devices with boron anode junction concentration of 1×10^{16} ions/cm², both junctions depth of 1.69 μm (Fig 5 a)) and 4.69 μm (Fig 5 b)) experienced the highest total current density of 3.0×10^{14} A/cm² (highest red color density) at P+ anode junction. The total current density is directly proportional to the electrical field [10]. Fig 5 a) shows the highest total current density occurring vertically across parallel plane while Fig 5 b) across the junction edge. Fig 5 c) represents the total current density doping profile distribution with lighter junction concentration of 5×10^{15} ions/cm² and junction depth of 4.69 μm . On the anode junction surface as shown in Fig 5 c), less than 3.0×10^{14} A/cm² total current density is observed. When the device experienced reverse bias condition, the junction breakdown results in a large voltage drop and a large current flows leading to the generation of heat.

The highest total current density areas observed in Fig 5 a) and b) behave as a heat spot, which causes junction damage by the thermal stress. On the other hand, less than $3.0 \times$

10^{14} A/cm² total current density is observed spreading uniformly across the surface of anode junction in Fig 5 c), which has lighter and deeper junction. . Hence, the lower electrical field is explained as spreading uniformly across the anode junction for this process split.

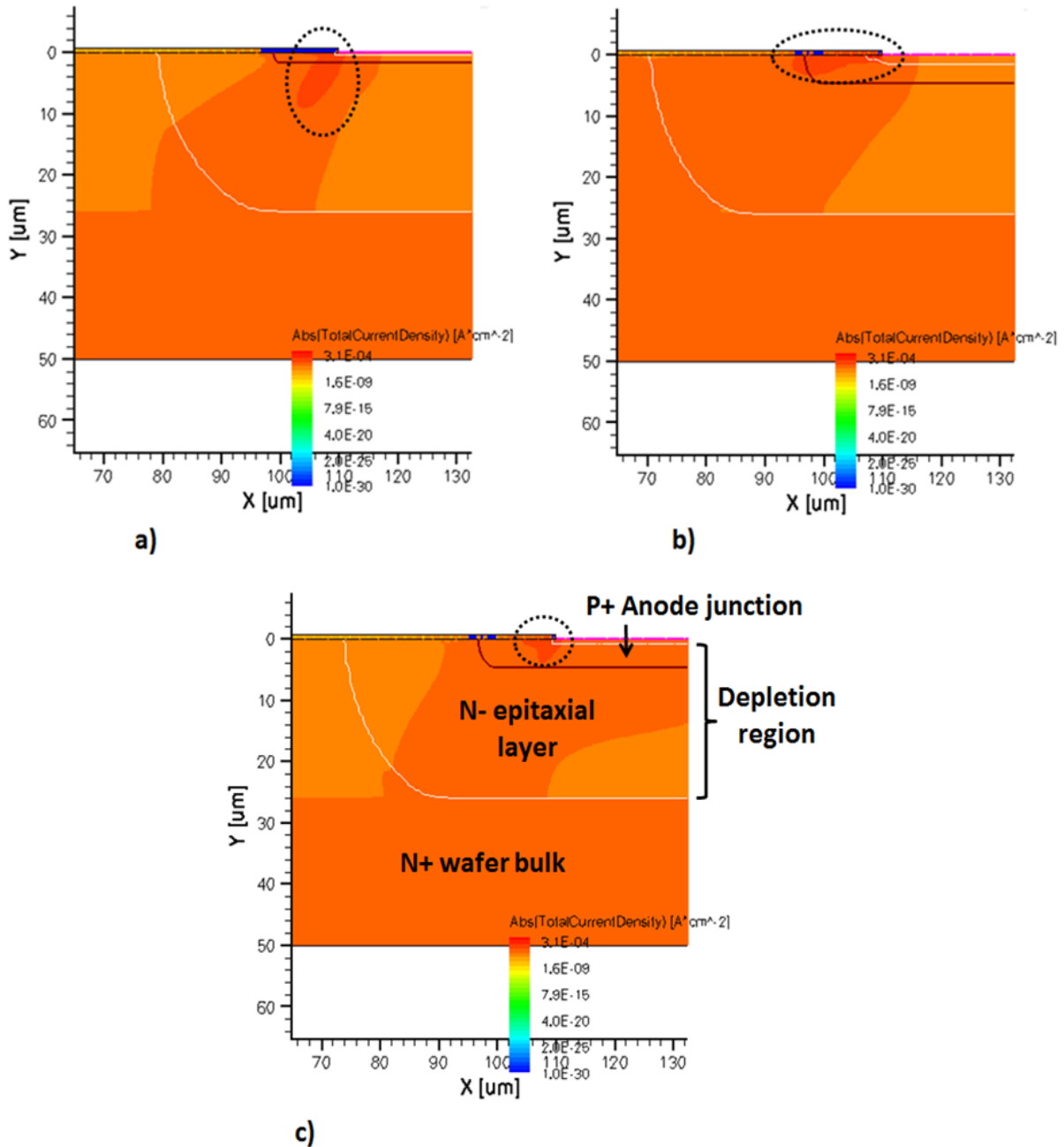


Fig 5: Total current density doping profile distribution of a) Control group: junction profile with 1×10^{16} atom/cm² and junction depth of 1.69 μm , b) Group a: junction profile with 1×10^{16} atom/cm² and junction depth of 4.69 μm and c) Group b: junction profile with 5×10^{15} atom/cm² and junction depth of 4.69 μm

The impact ionization is proportional to the electrical field [11]. Thus, the impact ionization doping profile distribution under reverse bias condition as shown in Fig 6 can be analysed. The dopant concentration of anode junctions in Fig 6 a) and b) are similar at 1×10^{16} ions/cm² but differ in junction depth, which are 1.69 μm and 4.69 μm , respectively. The highest impact ionization level of 3.5×10^{18} cm³/s indicated as highest red color density region, which circled in Fig 6. Based on the Fig 6 a), b) and c), comparison is made among

the 3 scenarios to see which of these have the preferable lowest impact ionization level occurring along P+ anode junction in contact with N- epitaxial layer.

Fig 6 a) shows that, at anode junction concentration of 1×10^{16} atom/cm² and junction depth of 1.69 μm , the highest impact ionization level is at the junction in the parallel plane. With the same anode concentration of 1×10^{16} atom/cm² and deeper junction depth of 4.69 μm , Fig 6 b) shows that the highest impact ionization level is at the junction edge. The high impact ionization, which occurs at the junction edges is less preferable due to a smaller surface area for heat dissipation, which causes inability of the device to withstand higher voltage supply during ESD surge test. The highest impact ionization levels observed in both Fig 6 a) and b) react as a heat spot, which leads to junction damage and metal spike by the thermal stress. Fig 6 c) shows the anode junction profile at lower concentration of 5×10^{15} atom/cm² and 4.69 μm junction depth. In contrast with the impact ionization doping profiles in Fig 6 a) and b), Fig 6 c) shows a lower impact ionization level of $< 3.5 \times 10^{18}$ cm³/s occurred along the anode junction contact with N- epitaxial layer, therefore enabled the junction to withstand higher voltage supply without any damage, metal penetration or metal spiking caused by thermal stress.

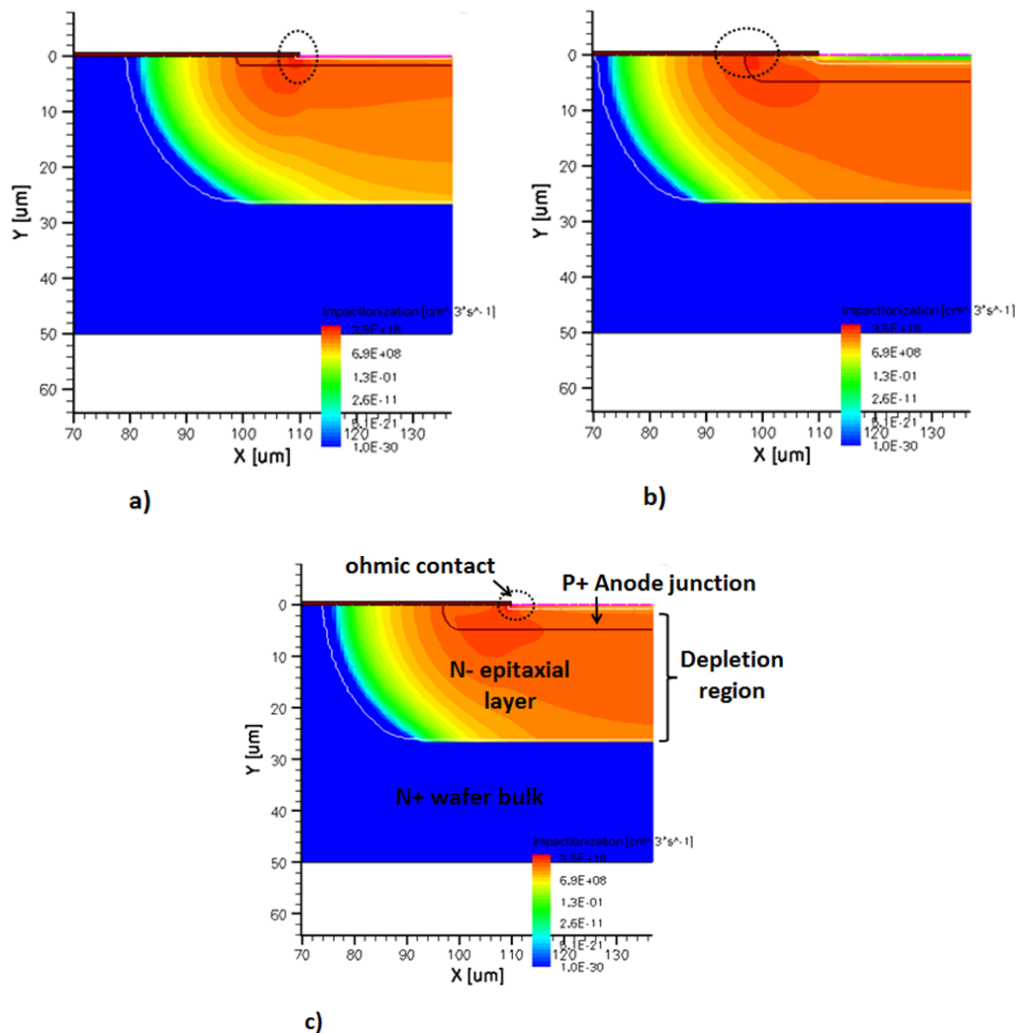


Fig 6: Impact ionization doping profile distribution of a) Control group: junction profile with 10^{16} atom/cm² and junction depth of 1.69 μm , b) Group a: junction profile with 10^{16} atom/cm² and junction depth of 4.69 μm and c) Group b: junction profile with 5×10^{15} atom/cm² and junction depth of 4.69 μm

By considering the result obtained from the total current density (Fig 5) and impact ionization simulations (Fig 6), further elaboration can be found in Fig. 7a (for shallow junction) and Fig. 7b (deeper junction). In both cases, during reverse bias, the P-i-N diode depletion region contour follows the edge as indicated by the dashed lines while the electrical field lines are indicated by the arrow lines. In area A, which is the P+ anode junction parallel plane, the electrical field lines are uniformly distributed. However, the electric field lines become crowded at the edge of junction as shown at area B. The electrical field is denser at junction edges compared to the parallel plane junction. As the electrical field increased, the total current density also increases [10], which leads to the degradation of ESD performance.

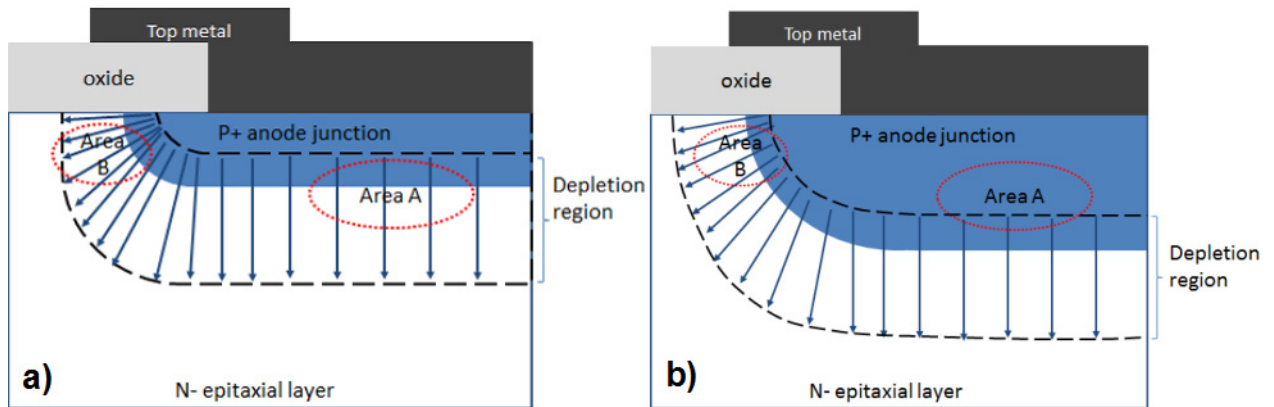


Fig 7: Junction breakdown mechanism for a) shallower junction planar diode, b) deeper junction planar diodes

Apart from the relationship between total current density and electrical field, the relationship between electrical field and impact ionization can be explained as well. By scaling down the chip dimension, the electrical field that occurs at the junction edges increases and therefore impact ionization plays an important role in device degradation due to hot-carrier effects and parasitic capacitance [12].

During reverse bias, the current tends to go through the anode junction edges, which are the weakest point [5]. This phenomenon results a high total current density and high electric field at anode junction edges, which limit reverse breakdown voltage and ESD performance. Several studies comparing the effects of the junction edges curvature with electrical field and the effects of junction edges curvature with total current density, are done using computational methods to perform field calculations on reversed-biased two-dimensional structures [13][14]. The theory is applied and being proved in the simulation result.

Based on the device physics theory, a lower electrical field can be created with a soft junction curvature. The maximum electrical field, which occurs at the anode junction edges is explained in the Equation 1 [5].

$$E_m(r_j) = \frac{qN_D}{2e_s} \left(\frac{r_d^2 - r_j^2}{r_j} \right) \quad (1)$$

where q is the electron charge, N_D is the donor concentration on the substrate, e_s is the dielectric constant of semiconductor, r_j is the junction depth and the depletion region extends into the lightly doped side to a radius r_d . Based on Equation 1, the increase of the anode junction depth (r_j), results in a decrease of the electrical field at the anode junction edges.

As illustrated in Fig 6 b), area B shows a reduction in the electrical field crowding effect by increasing the junction depth (r_j) when compared to a shallower junction planar diode shown in Fig 6 a). The reduction of electrical field crowding effect indicates a lower electric field and total current density.

In equation 1, the increase of the anode junction depth results in a lower electrical field at the junction edges. This is related to the depletion region width, which can be controlled by the dopant concentration of the anode junction [15]. Based on the simulation result and device physics theory, a lighter and deeper P+ anode junction profile can reduce the electrical field crowding effect at the junction edges. To increase the anode junction depth, a thermal diffusion process can be performed. However, the bigger the area of the junction, the larger the parasitic capacitance will be. There are two contributing factors to a diode's parasitic capacitance namely junction capacitance and diffusion capacitance[16]. The diffusion capacitance due to the injected carriers dominates under forward bias condition, while the junction capacitance is the capacitance associated with the charge variation in the depletion layer during reverse bias [16]. Therefore, the junction capacitance restricts the V_{BR} . The electrical performance varies with the alteration of the anode junction profile. Thus, a series of the design of experiment(DOE) was carry out to measure the deviation of the electrical performance.

b) Design Of Experiment Result

With the DOE as listed in Table 2, the output response of V_F , V_{BR} and I_R at the wafer level electrical test and ESD surge test (HBM and MM) at unit level, are observed. JMP variability charts are plotted to compare the electrical performance against the control group. Three major groups of A, B and C are shown in Fig 8, Fig 9 and Fig 10 with the black and blue distributions representing the evaluation and control groups, respectively.

Fig 8 shows the V_F under the forward current bias of 200 mA. All evaluation and control group distributions are below the maximum specification limit of 1.2 V. The V_F for evaluation groups shows a wider sigma when compared to the control group, due to wafer to wafer variations. Regardless of the boron pre-deposition process control variation, no significant difference is seen between the evaluation groups with drive in process temperature of 1200 °C and the control group with 950 °C process temperature. This is because the V_F variations of ± 50 mV between both groups are within the variations of production process and wafer substrates.

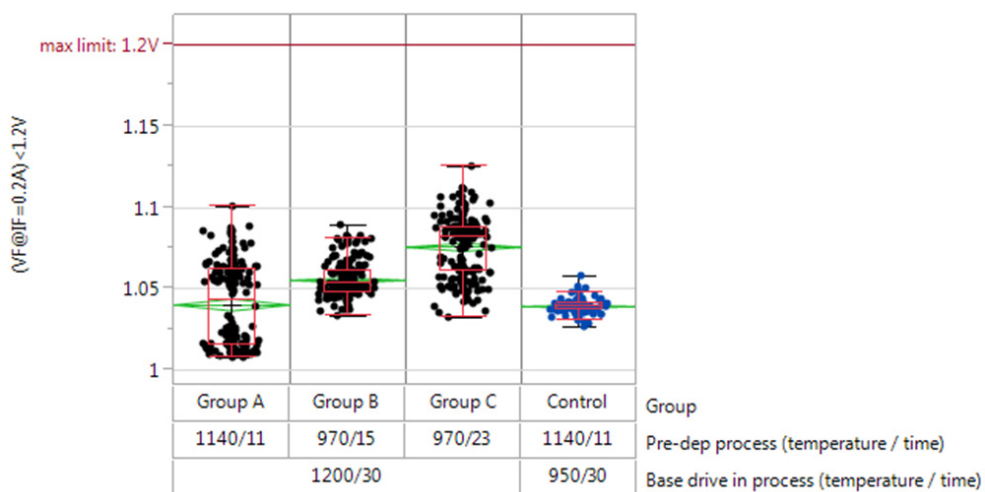


Fig 8: V_F wafer probe data @ 200mA

Fig 9 shows the V_{BR} under the reverse current bias of 5 μA . Both evaluation and control group distributions are above the minimum specification limit of 280 V. Based on V_{BR} wafer test data, by increasing the Boron drive in temperature from 950°C to 1200°C for Group A, B and C compared to control group, the mean V_{BR} value drops significantly. Higher boron drive in process temperature forms a deeper anode junction depth. In the P-i-N junction diode, a deeper anode junction reduces the epitaxial layer thickness. This reduction in epitaxial layer thickness results in a reduction of the reverse breakdown voltage as shown in Equation 2.

$$V_{BR} = E_C W_D - \frac{q N_D W_D^2}{2\epsilon_S} \tag{2}$$

From Equation 2, the V_{BR} is seen to be affected by the variable thickness of the epitaxial layer (W_D) [5][17][18][19][20].

In Fig 9, among the evaluation groups (A, B and C), Group A distribution shows the lowest V_{BR} with a mean of 305.45 V compared to Group B and C, with a mean of 322.67 V and 324.53 V, respectively. Based on Fig 9, we are only able to eliminate Group A process recipe combination for validation run as the V_{BR} is about 8.5% lower than the control group. All wafers from evaluation groups A, B and C are sent for device assembly and packaging for the ESD surge tests on HBM and MM.

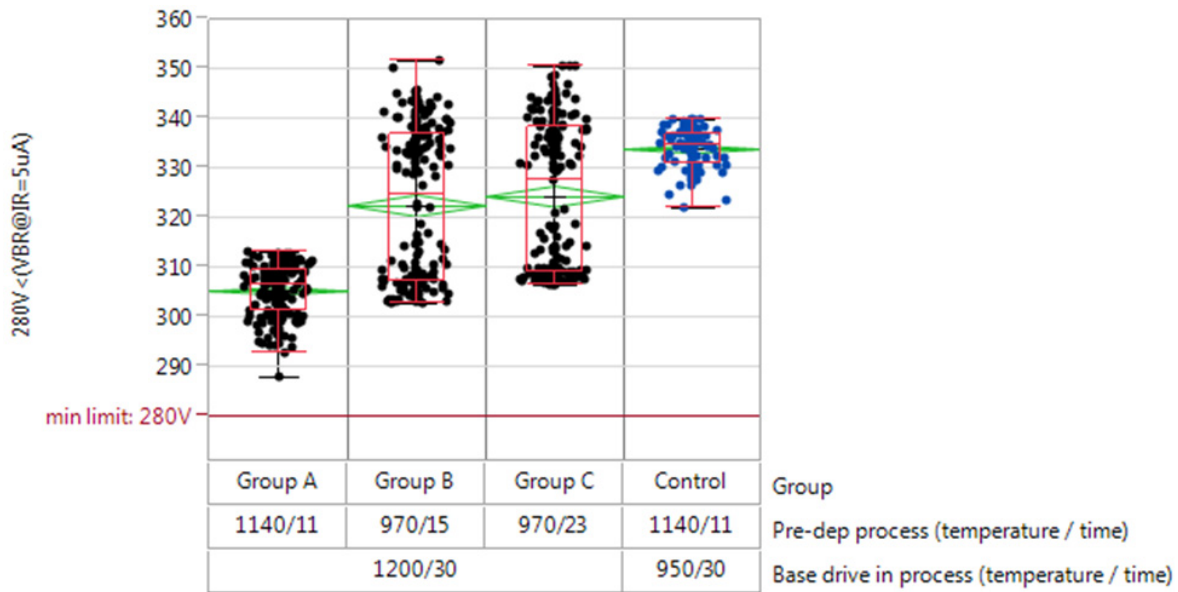


Fig 9: V_{BR} wafer probe data @ 5 μA

Fig 10 shows the I_R electrical performance under the reverse voltage bias of 260 V. In reverse bias, the purpose of having the I_R is to ensure the device performance breakdown at above 260 V without high leakage. Evaluation and control group distributions (group control, A, B and C) are obtained below the maximum specification limit of 500 nA. All groups did not show any significant difference as the reverse leakage current obtained is around 7 nA during 260 V reverse bias.

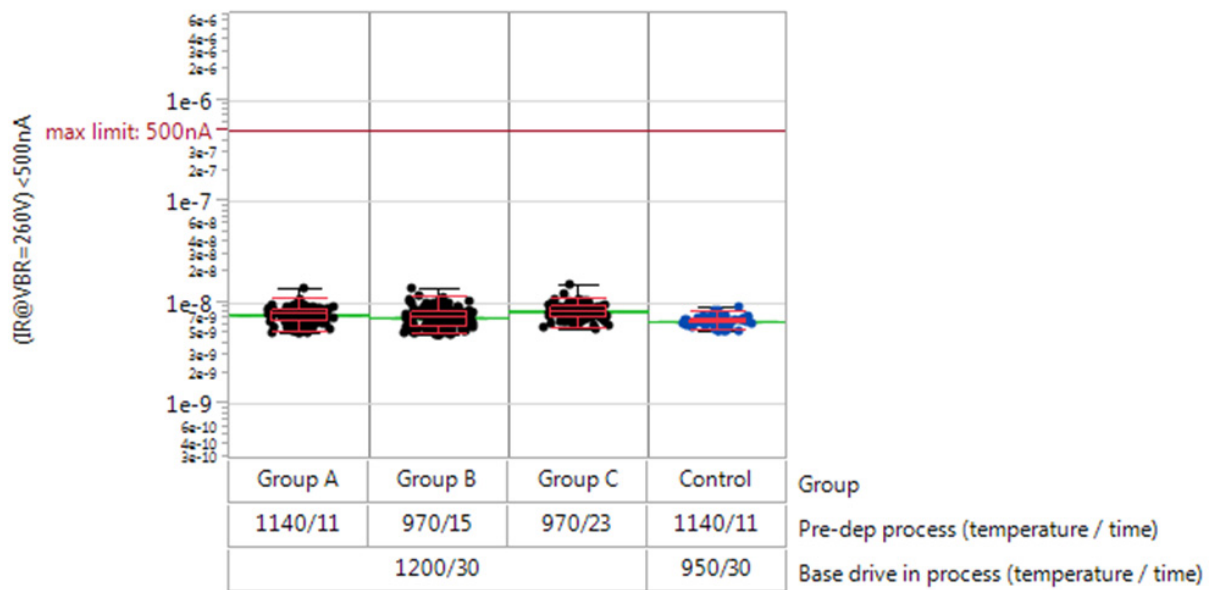


Fig 10: I_R wafer probe data @ 260V

Table 3: ESD result on evaluation lot in HBM and MM compared to control group

Group	ESD surge test	
	ESD HBM condition	ESD MM class
Control	250 ≤ failure < 500V	200V < failure ≤ 400V
Group A	1k ≤ failure < 2kV	Failure > 400V
Group B	1k ≤ failure < 2kV	Failure > 400V
Group C	1k ≤ failure < 2kV	Failure > 400V

Table 3 shows the ESD result on the evaluation groups (A, B and C) compared to control group in two types of ESD surge test model, which are ESD Human body model (HBM) and ESD Machine model (MM). Result shows that the improvement of ESD performance of all 3 evaluation groups (Group A, B and C) compared to the control group. Units from Group A, B and C are able to sustain the ESD voltage surge condition in the range of 1kV to 2kV for ESD HBM and exceed 400V for ESD MM while, the control group is only able to sustain ESD HBM surge in range of 250V to 500V and ESD MM surge in range of 200V to 400V.

In evaluation groups A, B and C, a higher oxide anneal in process temperature of 1200°C creates a deeper junction depth and thus softens the curvature of the junction edges. The deeper anode junction depth reduces the total current density and impact ionization resulting in a lower electrical field which occurs at the anode junction edges. Therefore, the deeper junction profile from evaluation groups allows a much more uniform heat dissipation and hence able to withstand higher voltage supply during ESD testing when compared to the control group.

As previously mentioned, this study is to choose the best boron pre-deposition and oxide anneal process combination with the improved ESD performance without any major deviation of V_F , V_{BR} and I_R at wafer level electrical performance. To choose the best process combination between groups A, B and C, a lower V_F , I_R and a higher V_{BR} are preferable. Based on the wafer test results shown in Table 4, all the evaluation groups did not show any significant difference on V_F and I_R electrical performance. In Table 4, group A can be

eliminated from the final process combination selection since the mean V_{BR} is 305.45V, marginally passes the minimum specification limit of 280 V.

Comparisons are made between groups B and C. In Table 4, no significant difference is observed in the electrical wafer test and ESD surge test output responses. Nonetheless, only group C process has been selected to be used in the subsequent qualification. The fixed process combination of boron pre-deposition process and boron junction drive in process condition is shown in Table 5.

Table 4: Summary table of DOE evaluation group compared to control group on mean value of electrical wafer test data and ESD surge test performance

Group	Mean value of electrical wafer probe data			ESD surge test	
	V_F @ 200mA	V_{BR} @ 5uA	I_R @ 260V	ESD HBM condition	ESD MM class
Control	1.04V	334.06V	6.873 nA	250 <= failure < 500V	200V < failure <= 400V
Group A	1.041V	305.45V	7.94 nA	1k <= failure < 2kV	Failure > 400V
Group B	1.056V	322.67V	7.496 nA	1k <= failure < 2kV	Failure > 400V
Group C	1.078V	324.52V	8.613 nA	1k <= failure < 2kV	Failure > 400V

Table 5: Final fixed Process changes for Group C

Group	Input response			
	Boron predeposition		Oxide anneal	
	Process temperature (°C)	Process time (mins)	Process temperature (°C)	Process time (mins)
Group C	970	23	1200	30

To test the process and wafer substrate variation, a total of 3 qualification lots with 6 wafers each have been selected to perform a same series of wafer fabrication process flow. After completing the 3 qualification lots, ESD results show that all qualification vehicles obtained improves ESD performance. ESD HBM was improved from Class 1A (250V<=failure < 500V) to Class 1C (1kV <= failure < 2kV) and ESD MM was improved from Class M3 (200V < Failure <=400V) to Class M4 (Failure < 400V).

Table 6: Summary table for ESD HBM & MM data

Qual vehicles	ESD HBM condition	ESD HBM class	ESD MM condition	ESD MM class
Control	250 <= failure < 500V	1A	200V < failure <= 400V	M3
Qual#1	1k <= failure < 2kV	1C	Failure > 400V	M4
Qual#2	1k <= failure < 2kV	1C	Failure > 400V	M4
Qual#3	1k <= failure < 2kV	1C	Failure > 400V	M4

4. Conclusion

Through the understanding of device behavior and performing the process of device simulation, the concept of creating a lighter and deeper depth of anode junction to improve the ESD performance of the 300V P-i-N power switching diode has been demonstrated. Based on the simulated results, a device with boron pre-deposition process of 970 °C for 23 minutes and annealing process at 1200 °C for 30 minutes is expected to withstand higher ESD. In the DOE, comparisons of different junction profile models have been carried out with a constant high boron drive in process temperature and different boron pre-deposition process controls, in order to achieve a deeper and lighter doped anode junction. Result shows an improvement in ESD performance for both ESD HBM and MM, similarly as expected in simulated results. Finally, qualification lots, which meet the requirement of the evaluation result are selected and fabricated with the fixed process combination of boron pre-deposition and anode junction drive in. All qualification samples meet the typical distribution electrical test specification of the commercial 300V P-i-N power switching diode device part, and have also shown an improved ESD performance.

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