Design of VD-DDCC for Novel Dual Mode Universal Filter with Grounded Passive Components

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ABSTRACT

This paper presents a novel dual mode multifunction filter using Voltage Differencing Differential Difference Current Conveyor (VD-DDCC) as active element. The filter provides low pass (LP), high pass (HP), band pass (BP), notch pass (NP) and all pass (AP) responses in voltage mode (VM) and transadmittance mode (TAM). The filter employs two VD-DDCC, two capacitors and three resistors. All passive components are grounded which is advantageous. The filters have the ability to operate in dual mode and don't require any capacitive matching. Quality factor of the filter can be tuned independent of the pole frequency. Input impedance for (VM & TAM) is high and output impedance for (TAM) is high as well. Double/negative voltage input signals for filter response realization are not required. The VD-DDCC and the filter circuit is designed and validated in Cadence Virtuoso Analog Design Environment using 0.18µm pdk from Silterra Malaysia at supply voltage of ± 1V. The achieved results are very close to the theoretical finings.

Keywords: Current Conveyor, Current Mode, Filters, VDDDCC.

1. INTRODUCTION

The current mode active elements are widely employed in designing universal frequency filters. The CM active elements exhibit greater linearity, wide bandwidth, simple structure, low power consumption and enhanced dynamic range [1-5]. Multitude of filters topologies using the CM ABBs has been demonstrated in the literature. But majority of the previously proposed filters can only operate in single mode i.e. current mode (CM), voltage mode (VM), transadmittance mode (TAM) and transimpedance mode (TIM). In present day intricate signal processing systems, the interfacing between CM and VM circuits is required. This task can be accomplished by TAM and TIM filters that not only perform signal processing but also provide interfacing between VM and CM systems. The development of mixed mode or dual mode universal filters that can provide low pass (LP), high pass (HP), band pass (BP), notch pass (NP) and all pass filter (AP) filter functions in CM, VM, TAM and TIM modes of operation are need of the hour.

Several exemplary filter topologies have been developed [6-16] that employ CM active elements but majority of them can function in single mode of operation only. Multi input single output (MISO) filter is one of the most used filter configurations. The filters proposed in [6-12] can only work in single mode of operation. The filters introduced in [6-9,13,15-16] employs more than two active elements for the design. The filter topologies given in [6,10] employs more than five passive components. The designs presented in [6,9-11,13,15-16] does not have inbuilt tunability property. The designs proposed in [10-11,13-14-16] require negative or double inputs to realize filter response. The literature review shows that most of the filters have one or more of the following drawbacks (i) can only function in single mode of operation (ii) no inbuilt tunability is

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provided (iii) employment of excessive number of active and passive components (iv) requirement of double or negative input signals.

This paper introduces a novel dual mode universal filter. The filter requires two VD-DDCC and five passive components. The filter employs all grounded passive components which is beneficial in noise cancellation and integrated circuit fabrication.

2. VOLTAGE DIFFERENCING DIFFERENTIAL DIFFERENCE CURRENT CONVEYOR (VD-DDCC)

The Voltage Differencing Differential Difference Current Conveyor (VD-DDCC) is a new active element that possess features of differential difference current conveyor (DDCC) and operational transconductance amplifier (OTA). Equations 1-4 give the voltage current (V-I) relations of the VD-DDCC and Figure 1 shows the block diagram of it.

$$I_W = I_{WC+} = -I_{WC-} = g_m(V_P - V_N) \tag{1}$$

$$V_X = V_{Y1} - V_W + V_{Y2} \tag{2}$$

$$I_X = I_{Z+} = -I_{Z-} \tag{3}$$
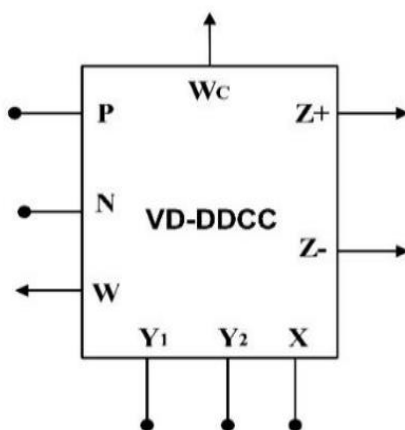
$$I_{Y1} = I_{Y2} = 0 \tag{4}$$

Figure 1. VD-DDCC Block Diagram.

The CMOS implementation of VD-DDCC is presented in Figure 2. The transistors M1-M13 forms the OTA section. The output current of the OTA assuming all transistors in saturation region and equal width and length for (M1-M2) will be $I_W = \pm I_{WC\pm} = g_m(V_P - V_N)$. The expression for g_m is given in Equation 5.

$$g_m = \sqrt{\mu_n C_{OX} \frac{W}{L} I_B} \tag{5}$$

where C_{OX} is the gate oxide capacitance, μ_n is the mobility of electrons in NMOS, g_m denotes the transconductance of OTA set via bias current I_B and $\frac{W}{L}$ is the aspect ratio of the transistors. Extra copies of the OTA current can be utilized, if necessary, for the applications. The second stage comprising of transistors M15-M32 provides algebraic summation of input voltages and current transfer function. The voltage at the X terminal is the algebraic sum of voltages at W, Y_1 and Y_2

terminals. The input current at the X terminal appears at the Z+ and Z- terminals, multiple copies of the current can be easily generated just by adding two extra transistors. The N, P, Y_1, Y_2 terminals are high impedance voltage input terminals. The W, W_{C+}, W_{C-}, Z + and Z − are high impedance current output terminals. The X terminal is low impedance current input terminal.
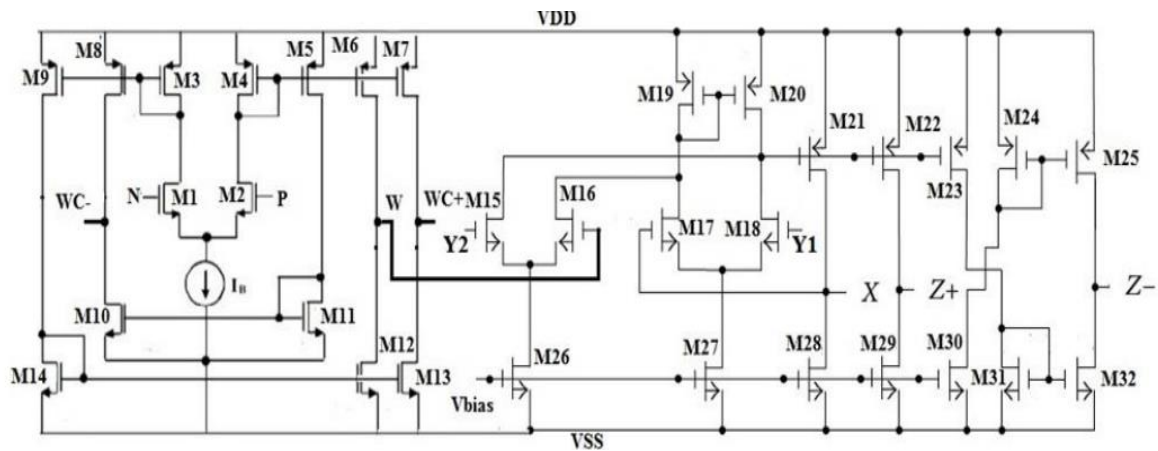

Figure 2. VD-DDCC CMOS implementation.

2.1 Proposed Electronically Tunable Dual Mode Universal Filter

Figure 3 shows the proposed filter. The filter consists of two VD-DDCC, only two capacitors and three resistors. The filter employs minimum number of passive components. The important features of the filter are: (i) only grounded passive components are used (ii) minimum number of passive components are employed (iii) no capacitive matching needed (iv) high input impedance in VM and TAM configuration (v) capability to get all five filter responses in VM and TAM modes of operation simultaneously (vi) explicit current output is available from high impedance node in TAM (vii) no double/negative voltage input signals required to generate filter responses (viii) inbuilt tunability. The Operation of the filter in the two modes is explained below.
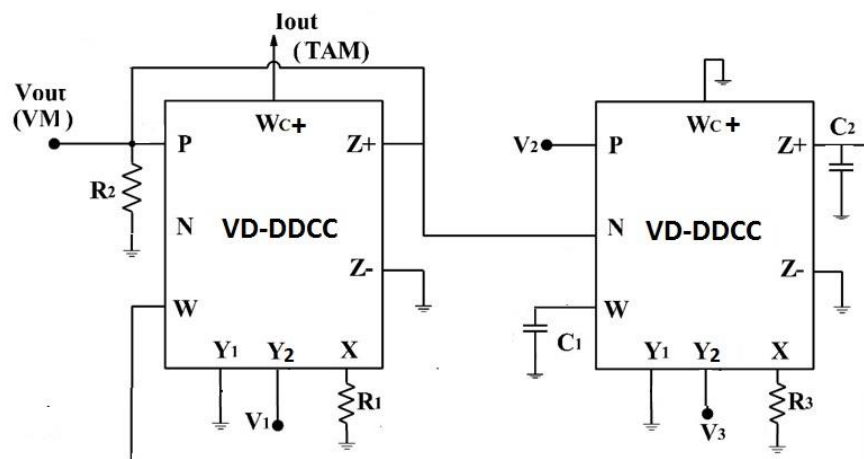

Figure 3. Proposed Mixed-mode Filter

In VM and TAM mode of operation, the filter is excited with input voltages $(V_1 − V_3)$ as per the sequence given in Table 1. The Equations (6-7) gives the filter transfer function in VM and TAM modes of operation. The frequency and quality factor are given by Equations (8-9). It can be deduced from the Equations that the Q can be controlled independent of frequency. For all pass response a simple resistive matching of $(R_1 = R_2)$ is required which is easy to achieve.

$$V_{out} = \frac{s^2 C_1 C_2 R_2 R_3 V_1 - S C_1 R_2 V_3 + R_2 g_{m2} V_2}{s^2 C_1 C_2 R_1 R_3 + g_{m1} S C_1 R_3 R_2 + R_2 g_{m2}} \tag{6}$$

In Equation 6 the filter gain constants are $H_{oLP} = 1$, $H_{oHP} = \frac{R_2}{R_1}$, $H_{oBP} = g_1 R_2$ by adjusting these parameters the filter gain can be adjusted. As special case for notch pass or band reject realization if $R_2 > R_1$ then high pass notch (HPN) is obtained and if $R_2 < R_1$ low pass notch (LPN) response is obtained.

$$I_{out\,(TAM)} = g_{m1} V_{out}$$

$$I_{out\,(TAM)} = g_{m1} \left[\frac{s^2 C_1 C_2 R_2 R_3 V_1 - S C_1 R_2 V_3 + R_2 g_{m2} V_2}{s^2 C_1 C_2 R_1 R_3 + g_{m1} S C_1 R_3 R_2 + R_2 g_{m2}} \right] \tag{7}$$

$$f_o = \frac{1}{2\pi} \sqrt{\frac{g_{m2} R_2}{C_1 C_2 R_1 R_3}} \tag{8}$$

$$Q = \frac{1}{g_{m1}} \sqrt{\frac{C_2 g_{m2} R_1}{C_1 R_2 R_3}} \tag{9}$$

Table 1 Excitation Sequence for VM and TAM

| Response	Inputs			Matching Condition
	V_1	V_2	V_3	
LP	0	1	0	No
HP	1	0	0	No
BP	0	0	1	No
BR	1	1	0	No
AP	1	1	1	$R_1 = R_2, R_3 g_1 = 1$

3. RESULTS AND DISCUSSION

To validate and test the designed filter the VD-DDCC is designed in 0.18μm pdk from Silterra Malaysia at supply voltage of ± 1V. The width and length of used transistors are illustrated in Table 2. The bias current of the OTA of the VD-DDCC is set at 47μA leading to the transconductance of 500μS. The passive components of the filters are selected as $R_1 = R_2 = R_3 = 2$ kΩ, $C_1 = C_2 = 15$pF. According to Equations 8 and 9 the center frequency and the filter quality factor are found to be 5.3 MHz and 1 respectively.

**Table 2** Width and Length of the MOS transistors

Transistors	Width (μm)	Length (μm)
M1-M2	1.8	0.36
M3-M9	3	0.72
M10-M14	8	0.36
M15-M18	4.5	0.36
M19-M20	20	0.36
M21-M22, M23	17.5	0.36
M24-M25	17.5	0.36
M26-M27	13.5	0.36
M28-M29, M30	8.75	0.36
M31-M32	6.45	0.36

The AC analysis of the filter is carried out to examine the VM and TAM responses. Voltage mode responses of the filter are presented in Figure 4. The gain and phase responses of the AP in VM mode are show in Figure 5.
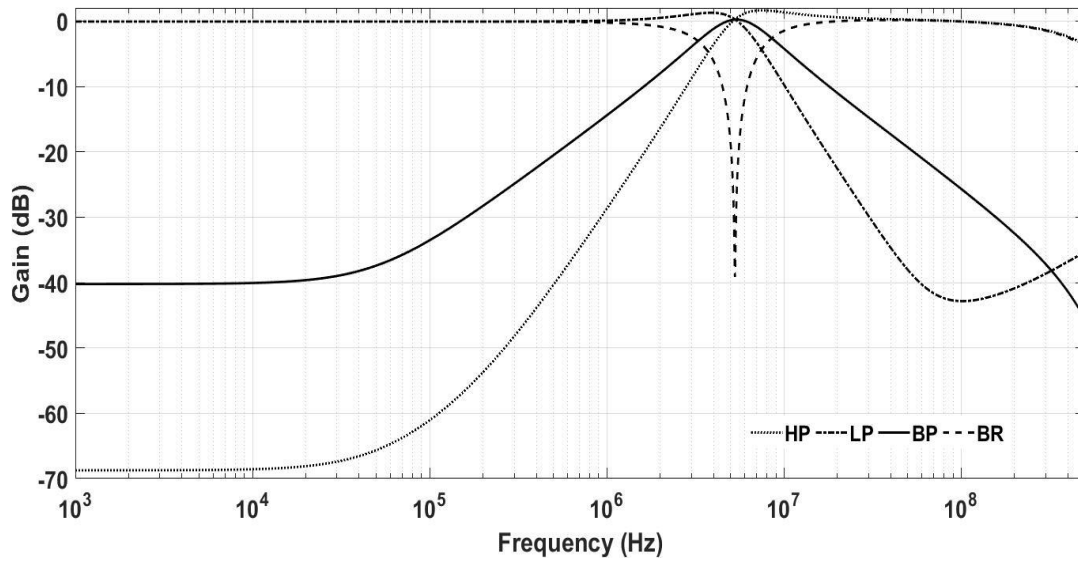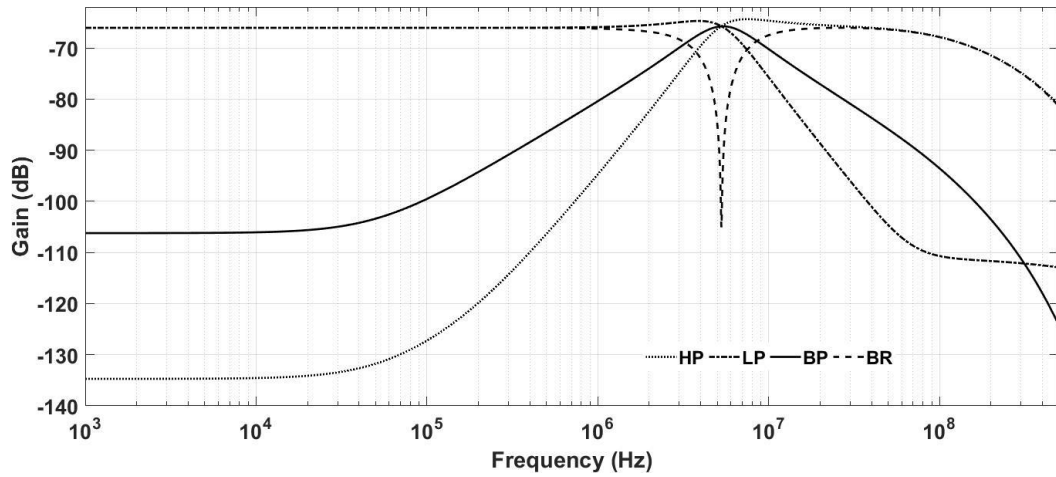

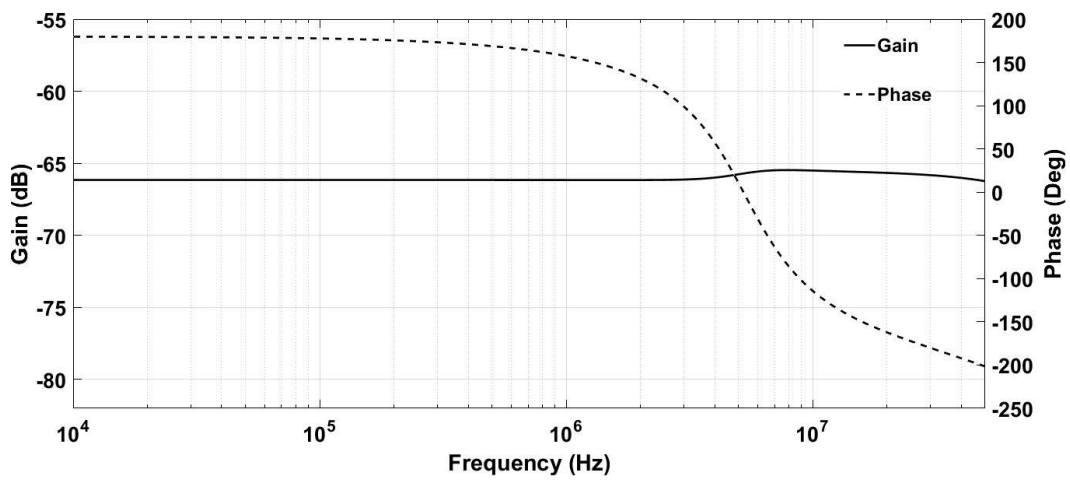**Figure 3**. VM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter.
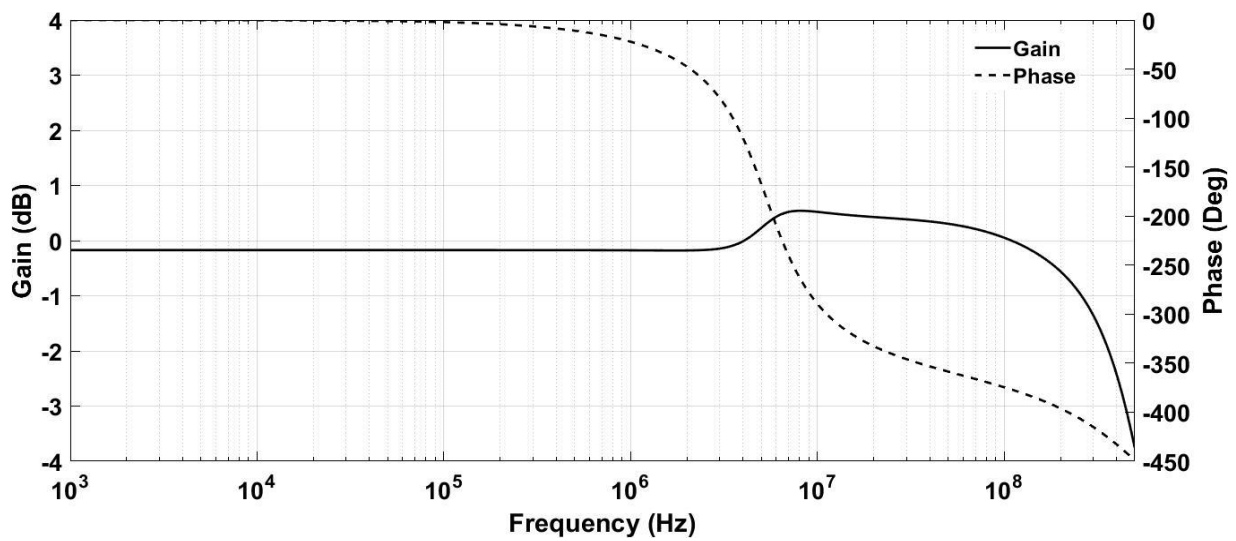
Figure 4. VM MISO configuration: Gain and phase responses of the AP filter.

The TAM mode responses are presented in Figure 6. The AP phase and gain responses are shown in Figure 7. The results proof that the filter structure performs correctly.

Figure 5. TAM MISO configuration: Frequency responses of the LP, BP, HP, and BR filter.


Figure 6. TAM MISO configuration: Gain and phase responses of the AP filter.

Transient analysis is used to test the signal processing capability of the proposed filter topology. A sinewave of 5.3 MHz frequency and 100mV amplitude is used and the LP, HP, BP and BR responses are monitored. It can be concluded from Figure 8 that the filter function correctly.
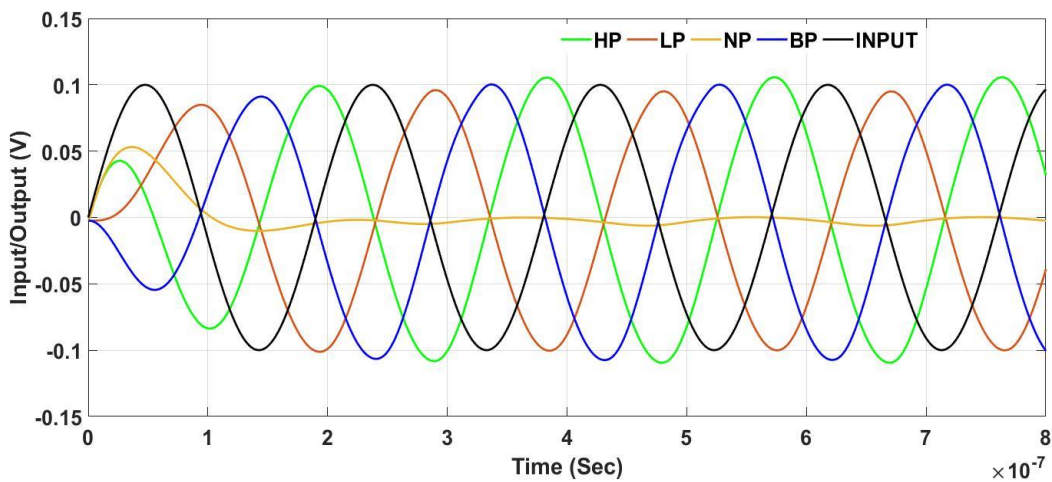

Figure 7. VM MISO configuration: Transient analysis results for BP, HP, LP filter configurations.

To study the effect of process spread on the performance of the designed filter Mont Carlo analysis is carried out for 200 runs. The Mont Carlo analysis results for VM AP response is shown in Figures 9.
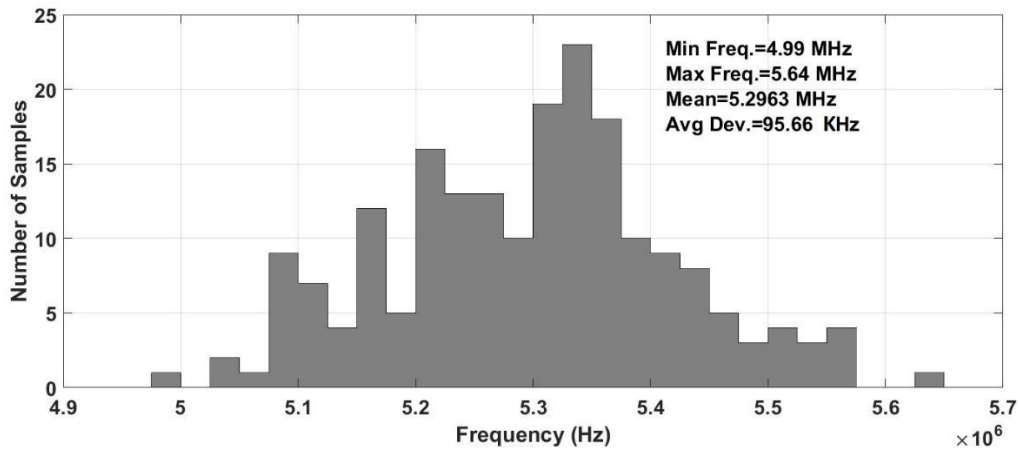
Figure 8. VM MISO configuration: The Monte Carlo analysis results for BP response.

In the presented filter the quality factor can be set independent of the pole frequency of the filter. The tunability of the quality factor is verified by analysing BP response in VM mode for different values of bias current IBIAS1 as shown in Figures 10. It can be deduced from figure that the quality factor of the filter can be tuned independent of the frequency.
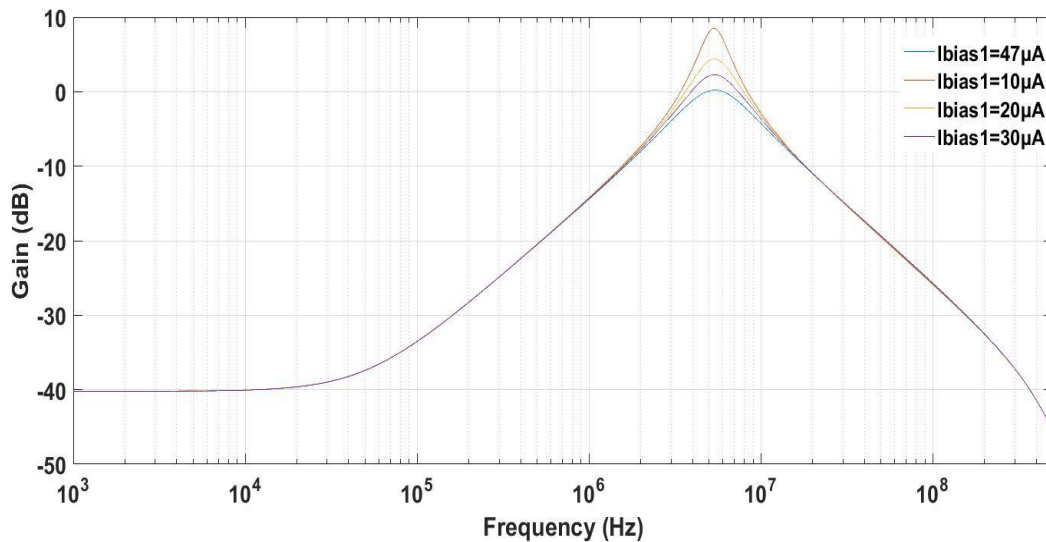
Figure 9. VM MISO configuration: Quality factor tuning for different values of OTA bias current in BP filter.

4. CONCLUSION

This paper introduced a novel dual mode multi-function universal filter. The filter employs two VD-DDCCs, three grounded resistors and two grounded capacitors. Presented MISO filter has inbuilt tunability and can realize all five filter responses in VM and TAM modes of operation. The VD-DDCC is designed in Cadence Virtuoso software and extensive simulations are carried out to examine and validate the proposed filter. The Monte Carlo analysis shows that the frequency deviation of the filter is within acceptable limits. The results validate the theoretical predications.

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