# Si-quantum Dots (QD) and SiO2 Tunnel Barriers

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## 1. Introduction

Oxidation of Si for nanostructures on silicon-on-insulator (SOI) substrates is a key process in the fabrication of Si single electron transistor (SET). The most difficult aspect of the fabrication process is the formation of a nanometer-scale island sandwiched between two small capacitors having a very thin insulator to allow electrons to pass through in a stochastic process, known as PADOX. This oxidation creates an island sandwiched between two tunnel barriers which constitutes a SET. The constriction of Si causes automatic tunnel barrier formation between source–QD and drain-QD. The unique characteristics of PADOX arises from i) the suppression of oxidation by mechanical stress, and ii) the oxidation from below.

## 2. Experiments

In this study 100mm p-type SOI wafers are used as the starting material. Square shaped samples of 4 x 5 mm, with one of the edges cut as a marker, were used as the standardized samples for SEM or AFM characterizations. To remove organic and inorganic contaminants, the wafer is cleaned using standard RCA cleaning, and dried. The substrate is then heated up to 200ºC for 30 mins using a conduction hotplate, and cooled down to room temperature. Negative resist is then spun onto the substrate at 3000 rpm for 30 s. To improve adhesion, the deposited resist is pre-baked at 90ºC for 120 s and left to cool to room temperature. This is then exposed to electron beams for lithography (EBL), which had a spot size of 45 µm and field size of 200 µm,at 20kV. After developing and rinsing, The nanostructures are characterized with a scanning electron microscope (SEM) and atomic force microscope (AFM). The lateral etch rate is obtained by measuring the structural differences in SEM images before and after etching, via an inductively-coupled plasma (ICP) reactive ion etching (RIE). Rapid thermal processing (RTP) 5-20 s oxidation at 1000ºC shrinks the QD dimension to between 10–30 nm. The oxidation rate of Si is determined by i) measurement of a reference sample, ii) reconstruction measurement via AFM, and iii) measurement of nanostructure cross sections using TEM.

## 3. Results and discussion

Important aspects in QD SET fabrication via patterning are i) sharpness of the design, ii) control of development time, and iii) optimum thickness of the Si layer. Both source– and drain-QD's are spaced by a nanoconstriction, designed to be narrower than the QD diameter. Even after etching, the nanoconstriction remained smaller than the QD. Hence, QD size shrinking and the tunnel barrier generation are easily achieved using thermal oxidation. After image development, unexposed negative resist areas are removed from the Si layer while the exposed areas remain on the Si layer. As the area of the unexposed negative resist decreased, its bonding strength to Si increased significantly, which leads to difficulty in removing the resist. In order to solve this, stepped image development and use of hexamethyldisilazane (HMDS), are utilized. The results of the reconstruction method for the applied PADOX process are as shown in *Fig. 1*.

Comparing the diameter of the $SiO_2$-embedded-Si nanostructure with the diameter of the initial Si nanostructure, there is a width difference of about 44 nm. Etching of $SiO_2$ embedded in a Si nanostructure is accomplished by dipping the oxidized sample in buffered oxide etch (BOE) for 5 s, and the final dimension of the Si QD is 225 nm in diameter. Comparison between the before-oxidation Si QD diameter with the after-BOE-dipped Si QD diameter, a difference of 109 nm is seen. A simple reconstruction method for $SiO_2$-embedded-Si nanostructures is performed. Etched Si nanostructures are furnace oxidized for 5 min. The oxidized Si nanostructures are then dipped in BOE for 5 s and then dried before AFM characterization. In the AFM, the before-oxidation-nanostructure dimensions are compared to after-oxidation. It is observed that the initial diameter of the QD is 335.48 nm, the diameter of $SiO_2$-embedded-Si is 389.77 nm and the diameter of the BOE-dipped SiO2-embedded-Si is 286.59 nm. It is also found that the reduced QD depth is 48.89 nm which gives the approximate oxidation rate of 9.78 nm $s^{-1}$. QD Images of BOE-dipped samples are smaller in size than those of etched samples.

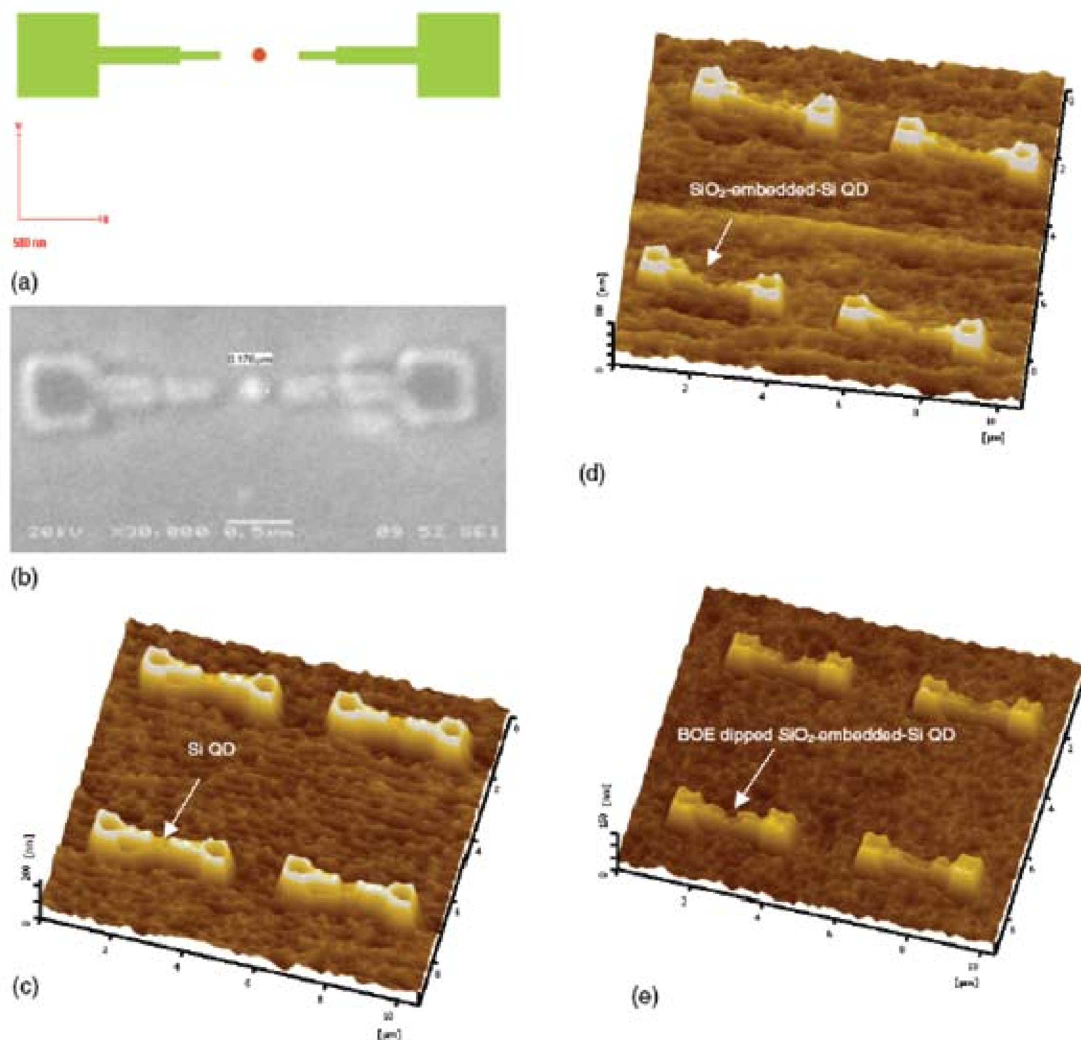


*Fig. 1* : (a) software designed source–drain and dot, square source–drain design width is 500 nm x 500 nm, and diameter dot is 80 nm; (b) SEM image of exposed resist with a dot diameter of 176 nm and nanoconstriction widths of 149 and 90 nm; (c) AFM image of Si nanostructure with a QD diameter of 334 nm; (d) AFM image of nanostructure oxidized in a furnace for 5 min; (e) AFM image of QD array after BOE dip.

As etch time increased, the surfaces could be imaged more clearly under SEM. The furnace-oxidized-Si nanostructures are difficult to image and showed low contrast surfaces. Conversely, the RTP-oxidized-Si nanostructures are easy to image and showed high contrast surfaces. In general, the oxygen contents by weight (%) at the $SiO_2$ tunnel barriers are higher than those at the center the of Si QD. The oxygen contents in the RTP and furnace samples are approximately the same. These results show that oxygen diffusion has occurred. At the farthest distance from the center of the Si QD, the oxygen content diminishes and shows the substrate. Therefore, the approximation of the Si oxidation rate in the furnace is 0.1 $nms^{-1}$. On the other hand, after oxidation, the remaining average Si thickness is 43.35 nm. Therefore, the approximation of the Si oxidation rate in the RTP is 2.16 nm $s^{-1}$. From both oxidation results, the Si oxidation rate using RTP is higher than the Si oxidation rate using the furnace, and samples oxidized using RTP have a higher contrast surface and are more easily imaged under SEM. The total dimension of the $SiO_2$-embedded Si QD is about 63 nm in diameter.

## 4. Conclusions

A successful optimization of the oxidation process to shrink Si QD dimensions and grow $SiO_2$ tunnel barriers has been demonstrated. The RTP-oxidized samples are easier to image under SEM than the furnace-oxidized samples, and also the oxidation rates of the RTP-oxidized samples are higher than the oxidation rates of those of the furnace-oxidized samples. To determine the oxidation rates of Si nanostructures, destructive tests using TEM has accurate data than the reconstruction method. The compositions of $SiO_2$ tunnel barriers show relatively good quality and is agreeable for single-electron fabrication.

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